GX540

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER I EXAMINATIONS, 2000/2001

FIRST YEAR BIOMEDICAL ENGINEERING
FIRST YEAR ELECTRONIC ENGINEERING
FIRST YEAR ELECTRONIC AND COMPUTER ENGINEERING
FIRST YEAR INDUSTRIAL ENGINEERING
FIRST YEAR INFORMATION TECHNOLGY
FIRST YEAR MANAGEMENT ENGINEERING
FIRST YEAR MECHANICAL ENGINEERING
FIRST YEAR UNDENOMINATED ENGINEERING
SECOND YEAR BIOMEDICAL ENGINEERING
SECOND YEAR INDUSTRIAL ENGINEERING
SECOND YEAR MANAGEMENT ENGINEERING
SECOND YEAR MECHANICAL ENGINEERING

FUNDAMENTALS OF ELECTRONIC ENGINEERING

Professor L.E. Davis
Professor D. J. Wilcox
Mr. F. C. O'Malley

Duration of examination: *Two* hours

Instructions: Answer *four* questions

1. (a) (i) Describe in your own words the fundamental difference between a digital and an analogue electronic circuit. [2 marks]

(ii) List the seven basic digital logic gates and give the truth table for each gate. [7 marks]

(b) The circuit of figure 1 below shows a combinational logic circuit.

(i) Determine the Boolean expression describing this system. [3 marks]

(ii) Write down the truth table for this circuit. [3 marks]

(iii) Using the laws of Boolean algebra determine a simplified expression for the system. [5 marks]

(iv) Proceed to give an implementation of this expression using NAND gates only. [5 marks]

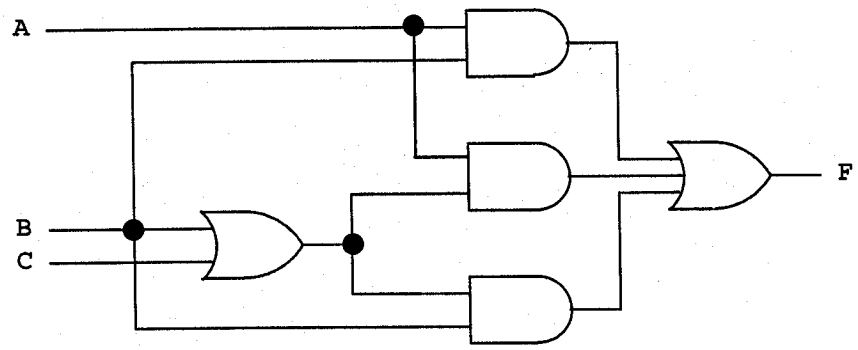

Figure 1.

2. (a) Using the laws of Boolean Algebra minmise the following expressions:

(i) $F = \left[A\overline{B}(C + BD) + \overline{AB}\right]C$ [4 marks]

(ii) $F = \overline{AB + AC} + \overline{AB}C$ [4 marks]

(iii) $F = A\overline{B}C(BD + CDE) + A\overline{C}$ [4 marks]

(b) Use Karnaugh mapping to minimise each of the following expressions:

(i) $F = \overline{A}\overline{B}C + \overline{A}B\overline{C} + AB\overline{C} + ABC$ [4 marks]

(ii)

$F = \overline{A}\overline{B}CD + \overline{A}B\overline{C}D + AB\overline{C}D + ABCD + AB\overline{C}\overline{D} + \overline{A}\overline{B}CD + A\overline{B}C\overline{D}$

[4 marks]

(c) Determine the Boolean logic expression described by the Karnaugh map below and give a circuit implementation of the expression:

Y	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	0	1	1	0
$\overline{A}B$	1	0	0	1
AB	1	0	1	1
$A\overline{B}$	0	1	1	0

[5 marks]

3. **(a)** Convert the following numbers to decimal clearly showing the conversion technique used in each case.

(i) 101100.10101_2 [3 marks]

(ii) $5C2_{16}$ [2 marks]

(iii) 7765_8 [3 marks]

(b) Convert each of the following numbers to hexadecimal format showing clearly the conversion technique used in each case.

(i) 100110000010_2 [2 marks]

(ii) 478_{10} [3 marks]

(iii) 47.07_8 [5 marks]

(c) Convert the following numbers to binary and perform the given arithmetic. Use 2's complement notation to perform the subtraction.

$(FD_{16} + 210_8) - 116_{10}$ [7 marks]

4. (a) (i) The diagram of figure 4.1 shows a sequential logic circuit which can act as a single bit memory element. Complete the truth table for this circuit, indicating all possible outputs Q_{n+1} for all possible combinations of inputs and previous outputs Q_n. [4 marks]

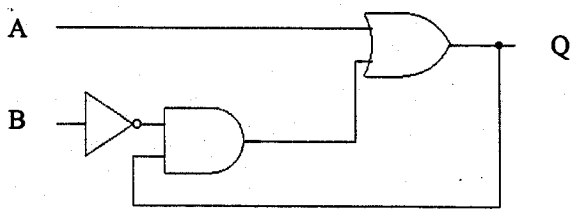

Figure 4.1

(ii) State which inputs **Set** and **Reset** the memory element. [2 marks]

(iii) State for which input combination is the device acting as a single bit memory. [2 marks]

(b) (i) Draw a circuit diagram for a *Gated D Latch.* [4 marks]

(ii) If the waveforms shown in figure 4.2 below are applied to the D and EN inputs of the gated D latch proceed to draw the corresponding output waveform Q. [6 marks]

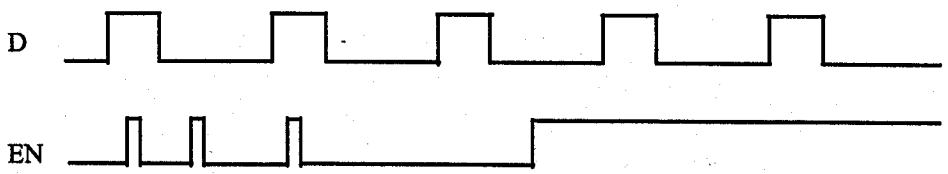

Figure 4.2

(c) Show how two S-R flip-flops can be connected together with any extra circuitry can be used to form a master-slave J-K flip-flop. [8 marks]

5. **(a)** **(i)** Draw a circuit diagram for a 3 bit asynchronous counter based on negative edge triggered JK flip-flops. [5 marks]

(ii) Explain why the counter is termed *asynchronous*. [2 marks]

(iii) Draw a timing diagram showing 8 complete clock cycles and all the corresponding flip-flop outputs. [5 marks]

(b) Design a synchronous binary counter to count in the following sequence:

0,1,2,3,4,5,6,7,0...

Your design should include truth table, state transition table, minimisation and logic circuit implementation.

[13 marks]

6. Answer any **TWO** parts.

(a) You are required to design a circuit that will cause the appropriate LEDs of a seven segment display to light based on a 4 bit BCD input WXYZ as shown in figure 6. Draw the truth table for the circuit and give minimal Boolean expressions for the segments a, b, c, and g. Proceed to give a circuit implementation for segment a only.

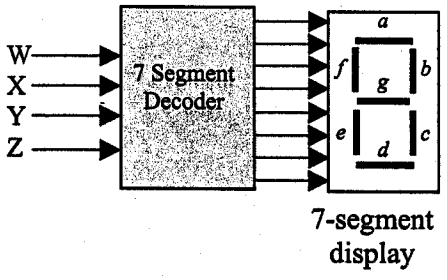

Figure 6

(b) **(i)** Explain the function of the following digital logic components:

Multiplexer, Demultiplexer [3 marks]

(ii) Give a logic circuit diagram for 4 – 1 data selector. [4 marks]

(iii) Show how it is possible to implement the following logic function using an 8 input multiplexer: $Y = \overline{A}_2\overline{A}_1A_0 + \overline{A}_2A_1A_0 + A_2\overline{A}_1A_0 + A_2A_1\overline{A}_0$

[5.5 marks]

(c) Draw the truth table for a full adder which will add two single bit numbers X and Y a and a input carry bit C_{in} to give sum and carry outputs S and C_{out}. Write down Boolean expressions for the two outputs and proceed to express them in minimal form. Give a circuit implementation for the adder based on the minimal expressions.

[12.5 marks]