GX544

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NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER I EXAMINATIONS, 2000/2001

SECOND YEAR ELECTRONIC ENGINEERING
SECOND YEAR ELECTRONIC AND COMPUTER ENGINEERING

DIGITAL SYSTEMS I

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Duration of Examination: ***Two*** **hours**
Instructions: Answer ***THREE*** questions
All Questions Carry Equal Marks

1. *(a)* Using Karnaugh mapping, design a circuit to implement the following function:

$$F(A, B, C, D, E) = \Sigma(0, 3, 7, 9, 11, 13, 15, 16, 25, 27, 29, 31)$$

(Your answer should include a circuit diagram to implement this function) **[10 marks]**

(b) Find a minimal sum of products expression for a prime number detector with five inputs, A, B, C, D and E, and a single output PRIME. The output should be high if the input is a prime number and zero otherwise. (You may assume that 0 is **not** a prime number). **[10 marks]**

2. Multiply the following signed numbers using Booths Algorithm: $15_{10} \times -13_{10}$ (assuming 5 bit 2's complement representation for the numbers)

You may use the following table to aid in generation of the partial product **[20 marks]**

x_i	x_{i-1}	**Action**
0	0	Shift **Partial Product** to the right and form the next **Partial Product**
1	1	Shift **Partial Product** to the right and form the next **Partial Product**
1	0	**Partial Product – Y**, then shift right
0	1	**Partial Product + Y**, then shift right

3. *(a)* Explain the following terms (i) Schmitt trigger input (ii) Propagation delay (iii) Open Collector **[9 marks]**

(b) With the aid of a circuit diagram, explain the operation of a two-input CMOS NAND gate. With the aid of appropriate equations, describe the main sources of power dissipation in CMOS devices. **[11 marks]**

4. Design an invalid count detector with two binary inputs and a single binary output. The output will remain high as long as the following pattern appears on the inputs: 00, 01, 10, 11, 00, etc. If the count is interrupted, the output goes low for the duration of the interruption. Use an ASM chart to describe the system, and use J-K flip-flops for its realization. **[20 marks]**

5. *(a)* Explain the following terms (i) Programmable Logic Device [PLD], (ii) Field Programmable Gate Array [FPGA], (iii) Application Specific Integrated Circuit [ASIC] **[6 marks]**

   (b) Show how the following function would be implemented on the PAL16L8 (See next page) **[14 marks]**

$$\overline{W} = AB\overline{CD} + AC + B\overline{D} + BCD$$
$$\overline{X} = \overline{A}BCD + ABC\overline{D} + \overline{B}\,\overline{C}$$
$$\overline{Y} = \overline{A}BD + \overline{A}\,\overline{C}D + AD + BC$$
$$\overline{Z} = ABCD + AB\overline{CD} + \overline{A}B\overline{CD} + ABD + \overline{A}\,\overline{C}D + BC\overline{D} + C$$

(Remember to include the completed PAL16L8 logic diagram [over] with your answer-book)