GX550

Ollscoil na hÉireann, Gaillimh

National University of Ireland, Galway

SEMESTER I EXAMINATIONS 2000/2001

THIRD YEAR ELECTRONIC ENGINEERING
THIRD YEAR ELECTRONIC & COMPUTER ENGINEERING

DIGITAL SYSTEMS II (EE316)

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Duration of Examination : **2 hours**

Instructions : Answer **THREE** questions.
All questions carry equal marks.

1. A pulse generator (debounce circuit) timing diagram is illustrated in figure 1(a). The system senses the state of the switch input [**sw(h)**] and, if high, asserts output signal **pls(h)** for exactly one clock cycle irrespective of how long **sw** remains asserted. The system does not allow additional assertions of signal pls until sw is first deasserted.

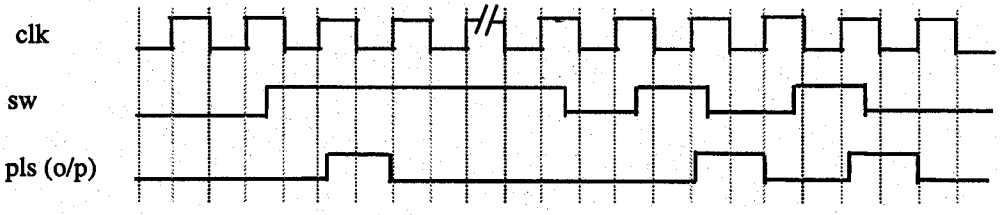


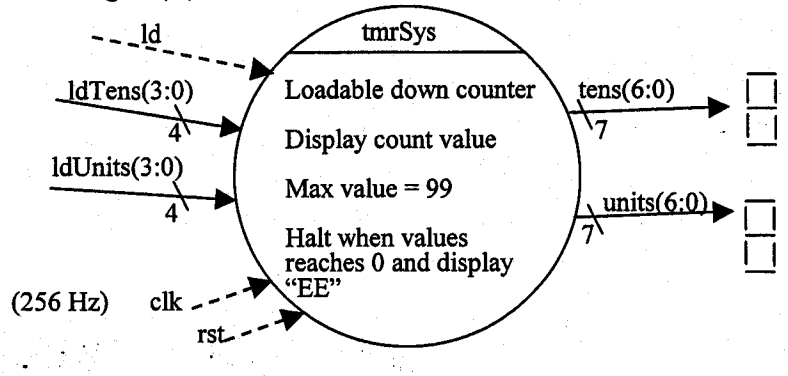
Figure 1(a) Sample timing diagram for Pulse Generator

a) Draw the flow chart describing the pulse generator system Finite System Machine (FSM) behaviour. (6 marks)

b) Re-draw the above timing diagram including your FSM state information (7 marks)
Note : a pullout page including figure 1(a) is included at the end of the exam paper for submission with the exam script.

c) Design and draw a gate level logic circuit to implement the flow chart functionality (7 marks)

2. Figure 2a illustrates the context diagram for a timer, which counts down each second from a maximum loadable value of 99 and displays the current count value on two seven segment displays. Count activity is halted when the count value reaches 0 and the display then shows 'EE'. An asynchronous reset switch stops all activity and resets the counter value (and hence display value) to 99. The system uses a 256Hz clock strobe (clk). Assume a pulse generator circuit element is already available to generate a synchronised pulse from input load signal (ld).



Data Dictionary for tmrSys Context Diagram

clk : system strobe. All synchronous element use this clk and are rising edge triggered
rst : asynchronous reset, asserted high. Resets counter value to 99.
ld : asynchronous load counter input. Assertion (h) loads the counter with the value on ldTens and ldUnits buses
ldTens(3:0) : 4 bit bus holding upper digit for loading in counter
ldUnits(3:0) : 4 bit bus holding lower digit for loading in counter
tens(6:0) : 7 bit bus representing 7-segment display bit pattern for upper digit of display
units(6:0) : 7 bit bus representing 7-segment display bit pattern for lower digit of display

Create a full and clear structured design documentation set i.e., context diagram, data flow diagrams, data dictionaries and functional partition to completely describe the timer system to a level from which a schematic database could be created. Include timing diagrams and truth tables as appropriate. List any assumptions made. Use synchronous design methods only (system clock = 256Hz throughout) (20 marks)

3. a) Figure 3a illustrates the Xilinx XC4k Configurable Logic Block architecture.
List the main features of this element and explain how combinational and sequential logic can be implemented in a CLB (4 marks)

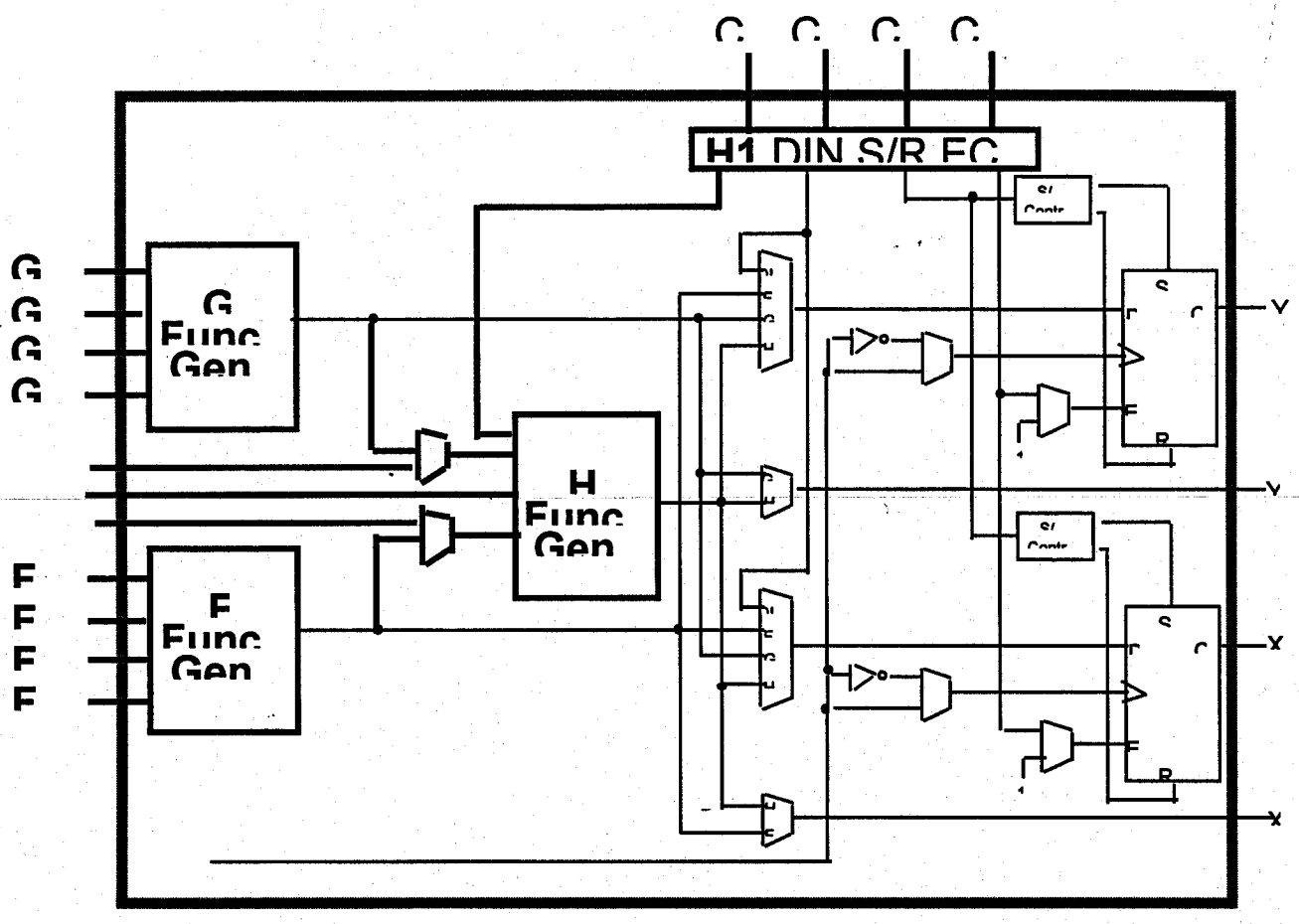


Figure 3a Xilinx XC4K FPGA Configurable Logic Block (CLB) Architecture

b) Figure 3b illustrates a functional partition for a synchronous up/down/loadable counter. Synchronous elements use a rising edge clock and all signals are high asserted.
Complete the timing diagram describing the operation of the system (fig 3(c))
Note : a pullout page including figure 3(c) is included at the end of the exam paper for submission with the exam script. (10 marks)

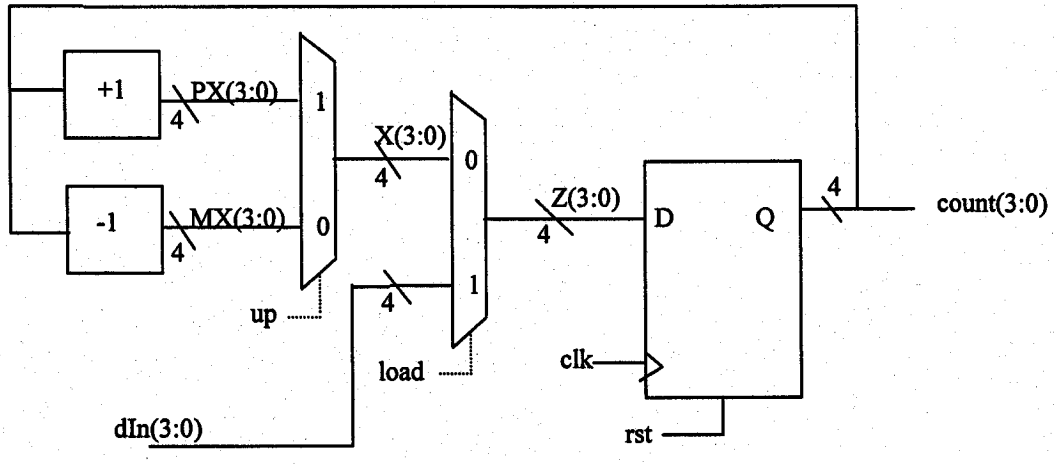


Figure 3(b) Counter system functional partition

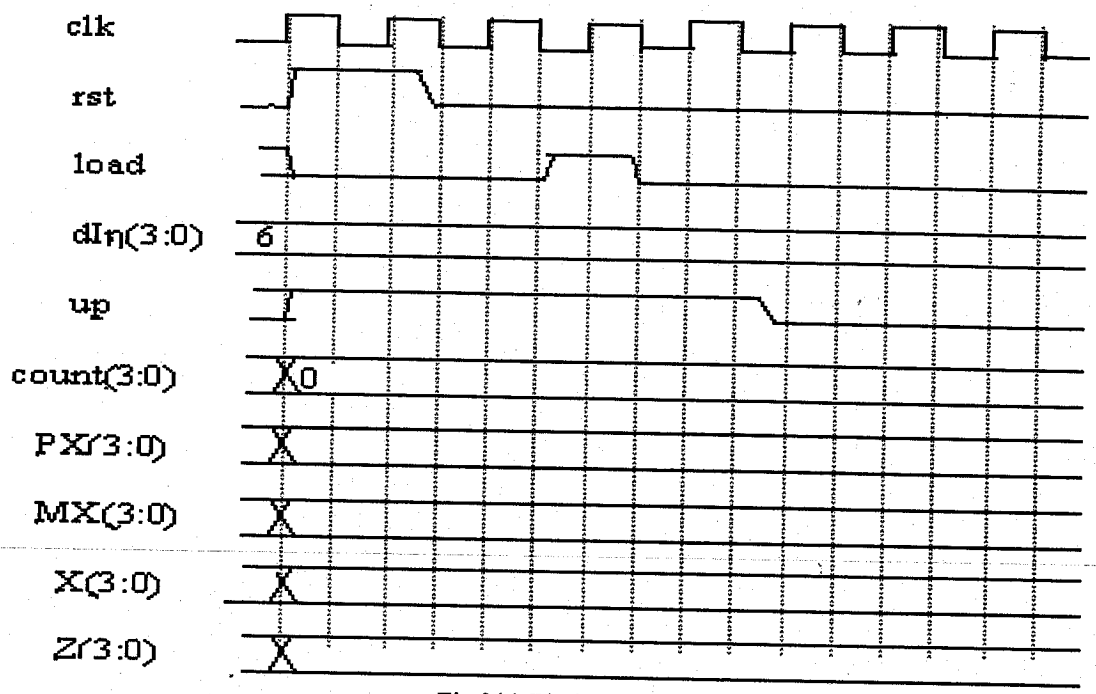
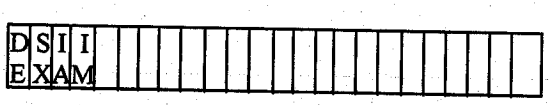


Fig 3(c) Timing diagram for Counter System

c) Write assembly code for the following function (5 marks)
Read 10 bytes of data starting at RAM address 40H and write data to PORT3 if the value is NOT EQUAL to ZERO. Use R3 as a pointer.

4. a) Write an 8051 assembly program to write the following text to a 20 character x 2 line HD44780-based LCD device. Use an 8-bit data interface, 2 line display and 5x7 font



Use a modular programming approach and include comments in code describing the operation of the LCD display. List any assumptions made. The HD44780 LCD instruction set is included as an appendix along with the ADuC812 Microconverter Quick Reference Guide. (13 marks)

b) Write an 8051 assembly program to trigger an interrupt every 0.8sec using an internal timer. Assume a 11.059MHz crystal frequency. Include clear comments in code explaining SFR bit settings and timer operation. (7 marks)