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THE NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS 2000

THIRD YEAR ELECTRONIC ENGINEERING EXAMINATION

ELECTRONIC DEVICES AND CIRCUITS

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Duration of Examination : **3 hours**

Instructions — Answer **FIVE** questions.
All questions carry equal marks.

1. An asymmetrical junction silicon diode has an extrinsic concentration of 10^{17} cm^{-3} on the N side and 10^{16} cm^{-3} on the P side. Under thermal equilibrium conditions at 27°C, calculate

a) the built-in potential across the space charge layer (6 marks)
b) the maximum electric field intensity inside the space charge layer(6 marks)
c) the distances the space charge layer extends into the P and N regions. (8 marks)

Boltzmann's constant, $k = 8.614 \times 10^{-5}$ eV/°K
Intrinsic carrier concentration (at 27°C) = 1.4×10^{10} cm^{-3}
$\epsilon = 11.8\epsilon_o$
$\epsilon_o = 8.854 \times 10^{-14}$ F/cm
$q = 1.6 \times 10^{-19}$ C

2. The circuit of figure 2 shows a typical common emitter amplifier.

(a) Calculate the d.c. operating point of the amplifier (3 marks)
(b) Draw the small signal model of the amplifier circuit (3 marks)
(c) Calculate the amplifier mid-band gain (5 marks)
(d) Choose capacitor component values to ensure that the low frequency cut off is < 50Hz (5 marks)
(e) Calculate the amplifier input and output impedances (4 marks)

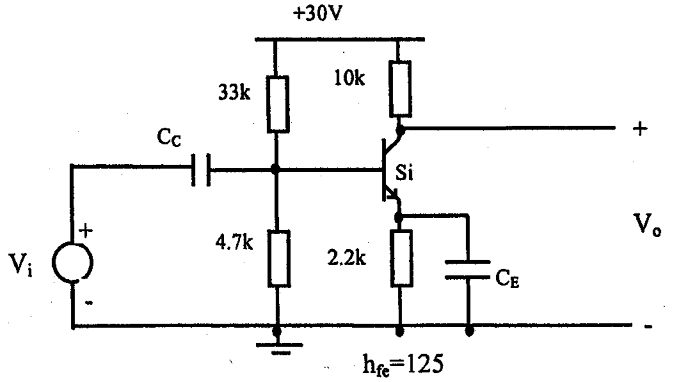


Figure 2 Common Emitter Amplifier

3. (a) In the circuit of fig 3, three sets of resistor values R1 and R2 are given as follows,

R1 = 80k and R2 = 2k
R1 = 8k and R2 = 20k
R1 = 80k and R2 = 20k

Which of the three alternatives would make the transistor potentially

(i) an amplifier (5 marks)
(ii) an open switch (5 marks)
(iii) a closed switch (5 marks)

Show appropriate calculations in your answer.

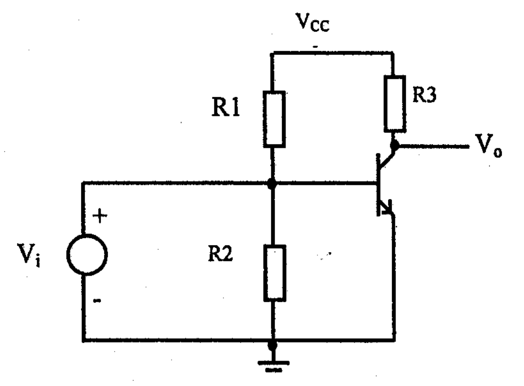


Figure 3 Transistor Circuit

(b) Discuss the factors which affect the bias point stability in a FET. (5 marks)

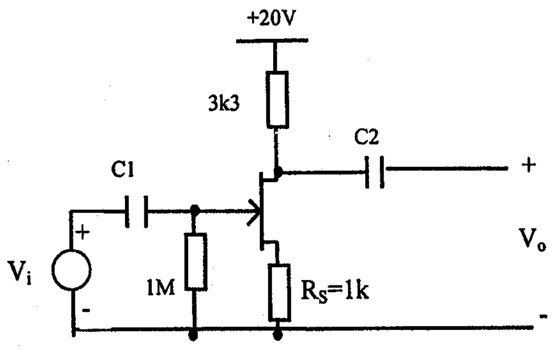
4. (a) List two characteristics of an N-channel JFET.
Sketch the I_{ds}-V_{ds} characteristic for an N-channel JFET, indicating the cut-off, linear and pinch-off/saturation regions of operation.
Illustrate the silicon behaviour of the JFET for each of the above operating regions. (3 marks)

(b) Repeat question 4(a) for an N-channel MOSFET device. (3 marks)

(c) Explain the role of the resistor in the source path of the FET amplifier circuit (figure 4) in stabilising the bias point of the amplifier (3 marks)

(d) Calculate the d.c. operating point of the FET amplifier (6 marks)

(e) Calculate the amplifier mid-band gain (5 marks)



I_{DSS}=8mA
V_{GSoff}=-6V

Figure 4 JFET Amplifier

5. (a) Design, using a zener diode a 10 volt regulated power supply to handle load currents of 0 - 500mA. The input voltage available is an unregulated supply which can vary over the range of 30-45 volts. You should allow at least 25mA zener current under worst-case conditions to ensure that the zener is operating in its active region (6marks)

(b) Calculate the maximum power dissipated in the zener and select a suitable power rating for this device. What are the main disadvantages of this simple zener regulator? (4 marks)

(c) The resistivity of pure germanium at a particular temperature is 52 ohm-cm. If it is doped with 10^{14} atoms/cm^3 of a trivalent impurity, estimate the new value of resistivity. Assume mobilities μ_n=3800cm^2/Vsec, μ_p=1800cm^2/Vsec and electronic charge q=1.6x10^{-19}C (10 marks)

6. (a) Explain what is meant by the term 'ideal' operational amplifier. Illustrate by explaining the operation of an op-amp based integrating amplifier circuit (5 marks)

(b) Figure 6 shows a temperature sensing circuit using a silicon sensor R_t. The sensor resistor has the following characteristics :

R_t = 825Ω at 0°C

R_t = 1.8kΩ at 100°C

(i) Calculate the value of R_x which gives V_o = 0V at 0°C (8 marks)

(ii) Calculate the value of V_o at 100°C (7 marks)

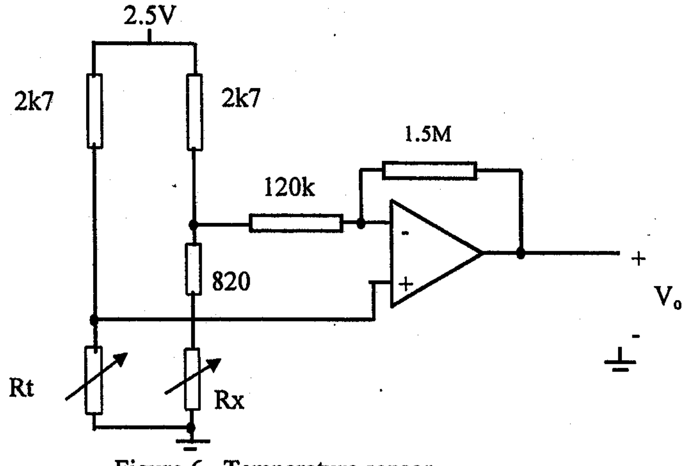


Figure 6 Temperature sensor

7. (a) Draw the circuit for a Schmitt trigger. Explain its operation and derive the input switching voltage values. (5 marks)

(b) Draw the circuit diagram of a differential amplifier and explain its principle of operation (include a current source in the emitters' circuit). (4 marks)

(c) Draw the small signal equivalent circuit model for a single ended differential amplifier and derive the expression for the small signal differential gain (6 marks)

d) Explain the following as they apply to operational amplifiers and illustrate (with waveform diagrams), the effect of each on the op-amp output signal. (5 marks)

(i) Input Offset Voltage

(ii) Slew rate

(iii) CMRR