GX559

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS, 2000

SECOND MECHANICAL ENGINEERING
SECOND BIOMEDICAL ENGINEERING

ELECTRONIC ENGINEERING

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Duration of examination: *Three* hours

Instructions: Answer *five* questions

1. Using Kirchoff's laws determine the voltage across the 2Ω resistor in the circuit of figure 1. By calculating the current drawn from each supply specify how much power is delivered to the circuit by the batteries. [20 marks]

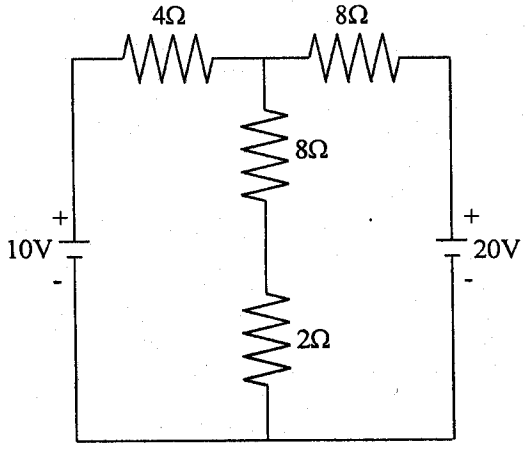

Figure 1.

2. (a) If a voltage v(t) = 100 sin(200πt) is applied across a 10kΩ resistor plot one cycle of the voltage and current and specify the rms values of each waveform. [2 marks]

(b) Derive the rms value of the half-wave rectified sinusoidal voltage waveform shown in figure 2.1. [8 marks]

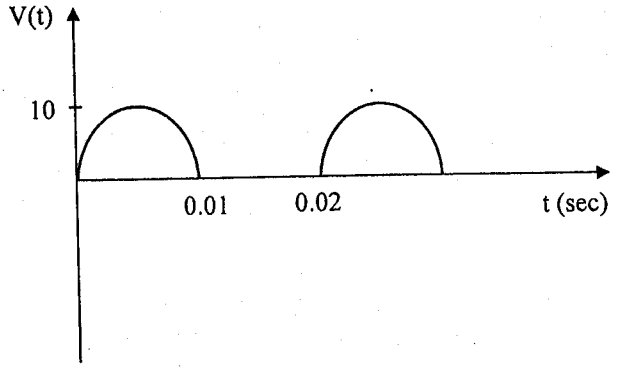

Figure 2.1

(c) The voltage waveform v(t) = 10sin(100 πt) is applied to the input terminals of the circuit of figure 2.2 Assuming an ideal diode, plot one cycle of both the output voltage and the current flowing in the resistor. [5 marks]

(d) Specify the average power delivered to the resistor. [5 marks]

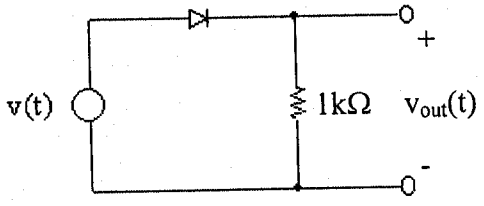

Figure 2.2

3. (a) Calculate the current in each branch of the circuit of figure 3 i.e. find $\mathbf{I_R}$, $\mathbf{I_L}$, and $\mathbf{I_C}$. [10 marks]

(b) Proceed to plot these currents on a phasor diagram and determine the magnitude of the supply current $\mathbf{I_S}$. [7 marks]

(c) Specify clearly the angle between the supply voltage and current. [3 marks]

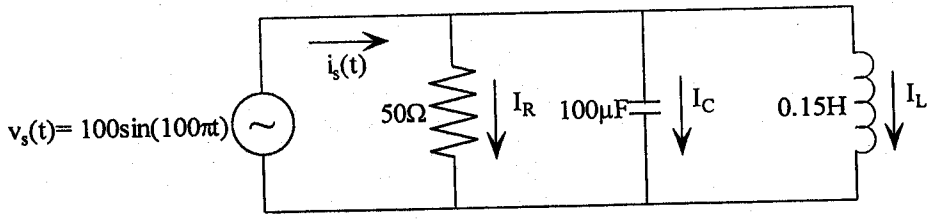

Figure 3.

4. (a) Show how it is possible to implement the function of the following:-

(i) A NOR gate using NAND gates only. [4 marks]

(ii) An X-OR gate using NOR gates only. [4 marks]

(b) (i) Determine the Boolean expression for the output Y of the circuit of figure 4. [4 marks]

(ii) Proceed to determine a minimal expression for Y. [4 marks]

(iii) Show how it is possible to implement Y using **NAND** gates only. [5 marks]

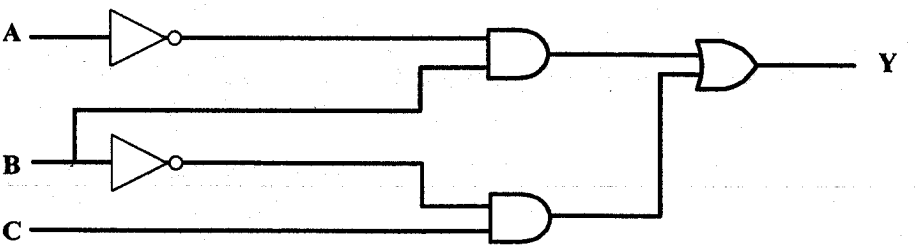

Figure 4.

5. (a) The circuit of figure 5.1 shows a gated S-R latch. Explain briefly the operation of this circuit and derive the truth table for the circuit for the condition **EN=1**. [9 marks]

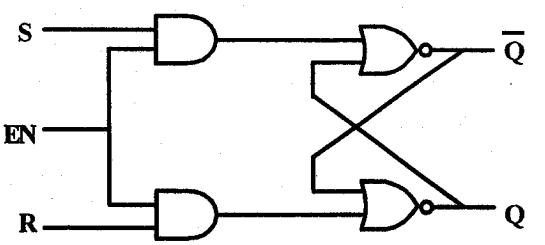

Figure 5.1

(b) Sketch the waveform for the output Q, if the inputs of figure 5.2 are applied to the above circuit. [6 marks]

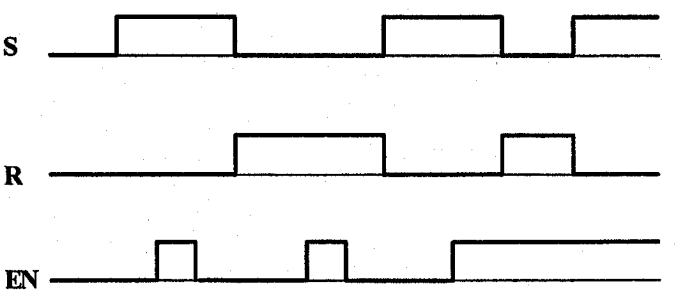

Figure 5.2

(c) Show how it is possible to extend the circuit of figure 5.1 to form a gated D-type latch. Explain how it possible to use a D-type latch to store one bit of information. [5 marks]

6. **(a)** Showing clearly the method used convert the following numbers to the base indicated.

(i) 678.14_{16} to decimal. [3 marks]

(ii) 705.12_{8} to binary. [2 marks]

(iii) 456.625_{10} to hexadecimal. [3 marks]

(b) Using the laws of Boolean Algebra reduce the following expressions to their simplest sum of products form.

(i) $\left(\overline{\overline{A}B\overline{C}+\overline{D}}\right)\left(D+\overline{C}A+1\right)+AB+\overline{A}B$ [3 marks]

(ii) $\overline{A}B\overline{C}D+ABC\overline{D}+A\overline{B}\overline{C}D+\overline{\overline{A}B\overline{C}D}$ [2 marks]

(c) Reduce the function F specified by the truth table of figure 6 to its simplest form using a Karnaugh map. Proceed to give an implementation of this circuit. [7 marks]

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Figure 6.

7. Answer any **TWO** parts.

(a) Design a synchronous sequential logic counter that will count in the following sequence: 2, 4, 6, 8, 2, ... etc. Your design should include truth table, and minimal circuit implementation using J-K flip-flops. [10 marks]

(b) Design a combinational logic circuit which will have two inputs A and B. Both A and B are two bit numbers. The circuit is to have a single output which will be HIGH if the product of the numbers A and B is odd. Note that Zero is considered odd. Your design should include a truth table, minimisation and circuit implementation. [10 marks]

(c) Draw the truth table for a half adder which will add two single bit numbers X and Y to give a sum and a carry output: S and C_{out}. Write down Boolean expressions for the two outputs and proceed to express them in minimal form. Give a circuit implementation for the adder based on the minimal expressions. Give a circuit that implements a full adder function with X , Y and C_{in} inputs and S and C_{out} outputs. [10 marks]