GX565

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS, 2000

FIRST ELECTRONIC ENGINEERING
FIRST ELECTRONIC AND COMPUTER ENGINEERING
FIRST YEAR INFORMATION TECHNOLOGY
SECOND INDUSTRIAL ENGINEERING

DIGITAL ELECTRONICS

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Duration of examination: *Two* hours

Instructions: Answer *four* questions

1. **(a)** Show how it is possible to implement the function of the following:-

(i) A NOR gate using NAND gates only. [4 marks]

(ii) An X-OR gate using NOR gates only. [4 marks]

(b) **(i)** Determine the Boolean expression for the output Y of the circuit of figure 1. [4 marks]

(ii) Proceed to determine a minimal expression for Y. [4 marks]

(iii) Show how it is possible to implement Y using **NAND** gates only. [5 marks]

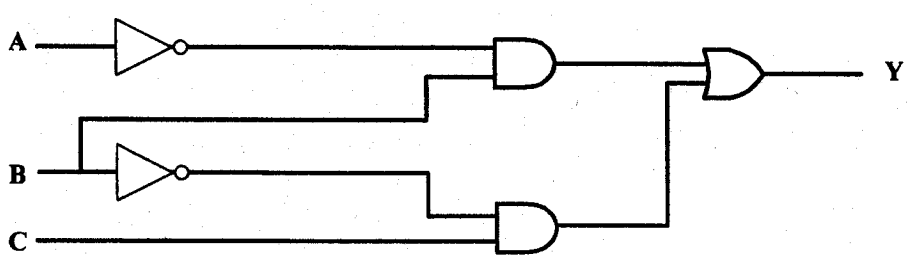

Figure 1.

2. **(a)** Using the laws of Boolean Algebra reduce the following expressions to their simplest sum of products form.

(i) $\left(\overline{\overline{A}B\overline{C}+\overline{D}}\right)\left(D+\overline{C}A+1\right)+AB+\overline{A}B$ [3 marks]

(ii) $\overline{A}B\overline{C}D+ABC\overline{D}+A\overline{B}\overline{C}D+\overline{\overline{A}\overline{B}\overline{C}\overline{D}}$ [2 marks]

(b) Determine the Boolean logic expression described by the Karnaugh map below and give a circuit implementation of the expression: [8 marks]

Y	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	0	0	1
$\overline{A}B$	0	1	1	0
AB	0	1	1	0
$A\overline{B}$	1	0	0	1

(c) Reduce the function F specified by the truth table of figure 2 to its simplest form using a Karnaugh map. Proceed to give an implementation of this function.

[7 marks]

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Figure 2.

3. (a) Convert the following numbers to decimal clearly showing the conversion technique used in each case.

(i) 10100111_2 [1 marks]

(ii) $3A5_{16}$ [2 marks]

(iii) 134.12_8 [2 marks]

(b) Convert each of the following numbers to hexadecimal format showing clearly the conversion technique used in each case.

(i) 10101010_2 [2 marks]

(ii) 578_{10} [3 marks]

(iii) 346.625_8 [4 marks]

(c) Convert the following numbers to 8 bit binary numbers and using 2's compliment notation calculate the value of Y.

$Y=145_{10} - 1F_{16}$ [6 marks]

4. (a) The circuit of figure 5.1 shows a gated S-R latch. Explain briefly the operation of this circuit and derive the truth table for the circuit for the condition **EN=1**.

[9 marks]

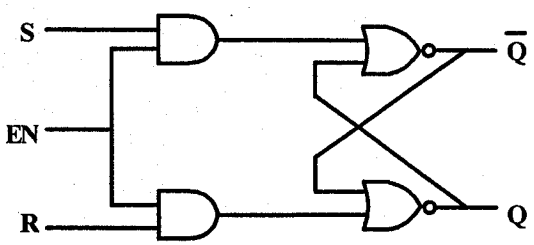

Figure 5.1

(b) Sketch the waveform for the output Q, if the inputs of figure 5.2 are applied to the above circuit. [6 marks]

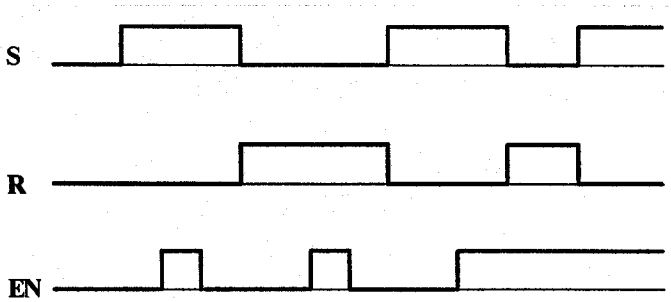

Figure 5.2

(c) Show how it is possible to extend the circuit of figure 5.1 to form a gated D-type latch. Explain how it possible to use a D-type latch to store one bit of information.

[5 marks]

5. You a required to design a combinational logic circuit for an automatic lawn sprinkler system. The circuit will be connected three sensors M, T and H and one input switch S which have the following function:

Sensor M: Moisture content of soil (M=1 if moisture content is high and M=0 if low).

Sensor T: Temperature (T=1 if temperature is high and T=0 if cool).

Sensor H: Humidity (H=1 if high humidity and H=0 for low humidity).

Switch S: Season indicator (S=1 during summer and S=0 otherwise)

The circuit is to have one output **A**, which when HIGH (A=1) will activate the sprinkler. The sprinkler is to be activated according to the following conditions:

Moisture content is low in winter *OR*
Temperature is high and moisture content is low during the summer *OR*
Temperature is high and humidity is high during the summer *OR*
Temperature is low and moisture content is low during the summer *OR*
Temperature is high and humidity is low.

Design the combinational logic circuit for the system, showing truth table, Karnaugh Mapping minimisation and circuit implementation. [20 marks]

6. Answer any **TWO** parts.

(a) Design a synchronous sequential logic counter that will count in the following sequence: 2, 4, 6, 8, 2, ... etc. Your design should include truth table, and minimal circuit implementation using J-K flip-flops. [10 marks]

(b) Design a combinational logic circuit which will have two inputs A and B. Both A and B are two bit numbers. The circuit is to have a single output which will be HIGH if the product of the numbers A and B is odd. Note that Zero is considered odd. Your design should include a truth table, minimisation and circuit implementation. [10 marks]

(c) Draw the truth table for a half adder which will add two single bit numbers X and Y to give a sum and a carry output: S and C_{out}. Write down Boolean expressions for the two outputs and proceed to express them in minimal form. Give a circuit implementation for the adder based on the minimal expressions. Give a circuit that implements a full adder function with X , Y and C_{in} inputs and S and C_{out} outputs. [10 marks]