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SUMMER EXAMINATIONS 2000

B.Sc. (Honours) Applied Physics and Electronics: Paper 1
B.Sc. (Honours) Physics and Computing: Paper 1

EP412: Digital Signal Processing

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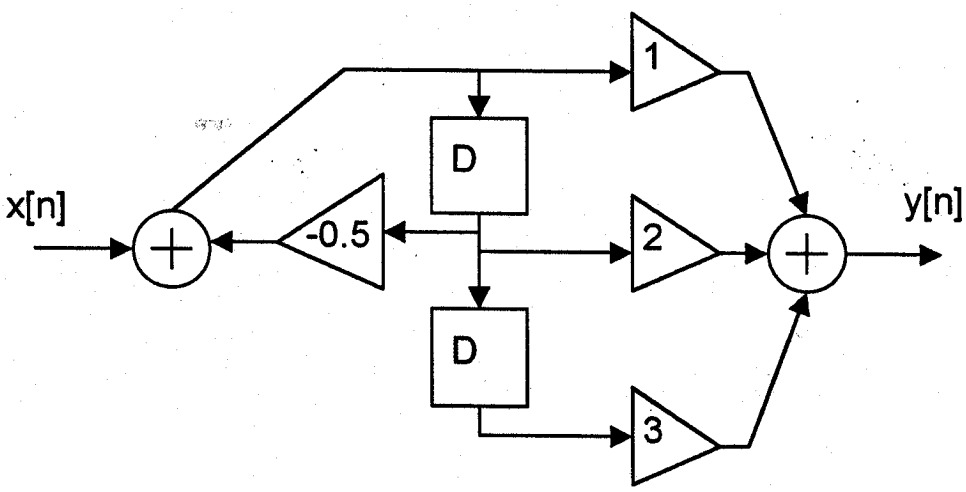
Time Allowed: TWO hours	Answer THREE questions

Q.1 Very briefly define or explain the following quantities as used in Discrete Time (DT) systems: (a) *the impulse response h[n];* (b) *the step response yu[n]; (c) the difference equation*; (d) *the transfer function H(z);* and, (d) *the Direct Form II (DF II) block diagram.*

The DFII block diagram for a DT system, with input x and output y, is shown in the diagram. Find the expression for the system transfer function H(z), identify its poles and zeros, and say whether the system is stable or unstable.



Hence find the system difference equation. Using this difference equation calculate the first 4 terms of the system impulse response h[n]. Write down the corresponding first 4 terms in the system step response.

Q.2 Say what is meant by a *digital filter*. State the relationship between the DT (Discrete Time) system function H(z) of a digital filter and its frequency response function. Explain how a pole-zero diagram of H(z) in the z-plane, together with the z-plane unit circle, can be used to estimate the filter frequency response.

Use the pole-zero technique, explained in the last part of this question, to sketch the approximate (qualitative) magnitude responses for the following filters:

(a) Two poles at $z = \pm 0.98j$, and two zeros at $z = -1$.
(b) One pole at $z = -0.9$ and one zero at $z = -1$.
(c) Five poles at the origin, one pole at $z = 0.9$, and one zero at $z = 0.9j$.

Q.3 Give a comparison of the BLT (Bilinear Transform) and II (Impulse Invariance) methods of DT system design, explaining how the BLT avoids the problem of aliasing. What is the disadvantage of the BLT approach compared to the II? How is this disadvantage partially overcome in practical design?

A DT resonator (band pass filter), with a sampling time $T = 20$ μsec, is to be designed with a resonant frequency of 10 kHz. Outline the steps in the procedure necessary to design the filter, working from a CT prototype H(s) and using the BLT (indirect design method).

Assume that H(s) is given once the CT resonant frequency and CT Q value are known. Calculate the required CT frequency numerically, but simply quote any relevant formulae (without calculations) to be used in the other steps of the design. How, qualitatively, will the Q value of the DT resonator differ from the value of Q in the CT original?

Q.4 Give a brief summary of the main hardware and software differences you would find between a specialised Digital Signal Processor (DSP) chip and a general-purpose microprocessor, such as a member of the INTEL Pentium series.

Using the technique of delay node variables d[n], set up the equations in d[n] and y[n] to solve the following difference equation:

$$y[n] + a_1 \cdot y[n-1] + a_2 \cdot y[n-2] = b_1 \cdot x[n-1] + b_2 \cdot x[n-2]$$

Write the TMS32010 assembly language code to solve the resulting difference equations in d[n] and y[n]. Assume the input x[n] is in Q15 form, that the filter coefficients (a, b) have been defined as Q12 fractions, and that y[n] is to be output in Q15 form. Neglect the problems of scaling and overflow.

NOTE: An abbreviated TMS32010 instruction set is appended to this paper.

Q.5 Answer any TWO of the following.

(a) Discuss the action and some of the drawbacks of practical ADC and DAC devices, as used in DSP systems. Your answer should include a description of sin(x)/x correction and quantisation noise.

(b) Describe the window method of indirect digital filter design, and explain its suitability for the design of linear phase filters. Why are such filters so desirable in practice?

(c) A DT system has the following difference equation:

$$y[n] - 0.5y[n-1] = x[n] + 2x[n-1] + x[n-2]$$

Find its system function H(z). Using H(z) find the first three terms in the system impulse response by the two distinct methods of
(i) a direct series expansion of H(z), and
(ii) a partial fraction expansion of H(z) followed by use of z-transforms.

Note that the z-transform of the DT series $x[n] = a^n$ is $\frac{1}{1 - az^{-1}}$.

A short TMS32010 Instruction Set

A 32 bit Accumulator

P = 32 bit Product register

T = 16 bit multiplicand register

Pan = I/O Port number n

d = Data memory address

S = Shift Left S bits

L = Label (address)

C = Constant

Mnemonic	Cycles*	Description
ABS	1	Absolute Value of A
ADD d,S	1	Add d (with shift) to A
AND d	1	AND d with A
APAC	1	Add P to A
B L	2	Branch unconditionally to label L
BGEZ L	2	Branch if A greater or equal to zero
BGZ L	2	Branch if A greater than zero
BIOZ L	2	Branch on BIO (I/O status) pin = 0
BLZ L	2	Branch if A less than zero
BLEZ L	2	Branch if A less than or equal to zero
BNZ L	2	Branch if A is not zero
BZ L	2	Branch if A is zero
CALL L	2	CALL subroutine L
DINT	1	Disable Interrupt
DMOV d	1	Copy contents of data memory d to next location
EINT	1	Enable Interrupt
IN d,PAn	2	Input data from I/O port n to d
LAC d,S	1	Load A from d (with shift)
LACK C	1	Load A with immediate 8 bit constant C
LT d	1	Load T from d
LTA d	1	Load T, add P to A (LT, APAC)
LTD d	1	Load T, add P to A, data move (LT, APAC, DMOV)
MPY d	1	Multiply d with T, store product in P
MPYK C	1	Multiply 13 bit constant C with T, product to P
NOP	1	No operation
OR d	1	OR d with A
OUT d,PAn	2	Output data from d to I/O port n
PAC	1	Copy P to A
RET	2	Return from subroutine CALL
SACH d,S	1	Store high order A (16 bits with shift) to d
SACL d,S	1	Store low order A (16 bits with shift) to d
SPAC	1	Subtract P from A
SOVM 1	1	Set Overflow Mode for A and ALU (±ve limits)
SUB d,S	1	Subtract d (with shift) from A
XOR d	1	Exclusive OR d with A
ZAC	1	Zero A

*** CPU cycle time:** TMS32010 = 200 ns