

Ollscoil na hÉireann, Gaillimh

National University of Ireland, Galway

SEMESTER I EXAMINATIONS 2000/2001

B.E. DEGREE IN ELECTRONIC ENGINEERING
B.E. DEGREE IN ELECTRONIC & COMPUTER ENGINEERING

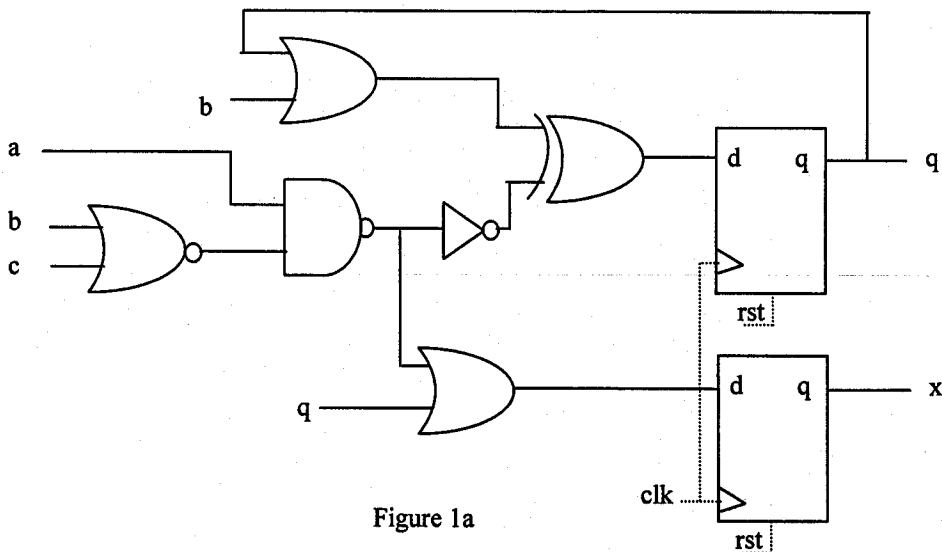
MICROELECTRONICS AND VLSI DESIGN (EE419)

Professor L.E. Davis
Professor D.J. Wilcox
Dr. F. Morgan

Duration of Examination : 2 hours

Instructions : Answer **THREE** questions.
All questions carry equal marks.

1. a) List the uses and benefits of VHDL. (3 marks)
- b) Write a VHDL entity and architecture description for the following sequential circuit (fig 1a). Use std_logic signals throughout. Assume asynchronous reset (rst) (8 marks)



- c) Draw the circuit diagram described by the following VHDL code (9 marks)
Indicate on the diagram the elements which make up each of the processes.

```
-- title & library
entity whatIsThis is
port (a,b,c,d,e,f : in std_logic; g : out std_logic);
end whatIsThis;

architecture rtl of whatIsThis is
signal x,y : std_logic;
begin

  procB : process (c, d, e)
  begin
    case e is
      when '0'    => x <= c;
      when others => x <= d;
    end case;
  end process procB;

  procA : process (a)
  begin
    if a'event and a = '1' then
      if b = '0' then
        y <= '0';
      else
        y <= x;
      end if;
    end if;
  end process procA;

  g <= (y and not x) when f = '1' else 'Z';
end rtl;
```

2. a) Detail the main steps in the VHDL synthesis process and action taken if synthesis fails. (3 marks)
- b) How many latches will the following VHDL code produce ? Explain. (4 marks)
Draw the synthesised circuit

```
entity entOne is
  port(en : in std_logic; a, b, c : in std_logic_vector(1 downto 0);
        d, e : out std_logic_vector(1 downto 0 ));
end entOne;

architecture rtl of entOne is
  signal
  begin
    process (a, b, c, en)
    begin
      if en = '1' then
        d <= a;
        e <= b;
      else
        d <= c;
      end if;
    end process;
  end rtl;
```

- c) Draw the flow chart or state transition diagram describing the following VHDL model
Include a flowchart key
(8 marks)

-- title & library

entity fsm is

port (clk, rst, a, b : in std_logic; kp : out std_logic;
end fsm;

architecture rtl of fsm is

type stateType : (idle, wait1, wait2);

signal CS, NS : stateType;

begin

SYNCH : process (clk, rst)

begin

if rst='1' then CS<=idle;

elsif clk'event and clk = '1' then CS <= NS;

end if;

end process SYNCH;

NS&OPDEC : process (CS, a, b)

begin

kp <= '0';

NS <= CS;

case CS is

when idle => if a='1' then NS <= wait1; end if;

when wait1 => if b='1' then

if a='1' then NS <= wait2; else kp <= '1'; end if;

end if;

when wait2 => if b='0' then NS <= idle; else kp <= '1'; end if;

when others => NS <= idle;

end case;

end process NS&OPDEC;

end rtl;

- d) Describe VHDL Testbenching and its uses.

(2 marks)

- e) Write VHDL testbench code describing a repeating strobe (clk) with 20ns period (3 marks)

3. a) Complete the timing diagram illustrating the behaviour of the circuit described by the following flowchart (fig 3a). Note : use and submit fig 3b timing diagram pullout page, attached at the end of the exam paper
(7 marks)

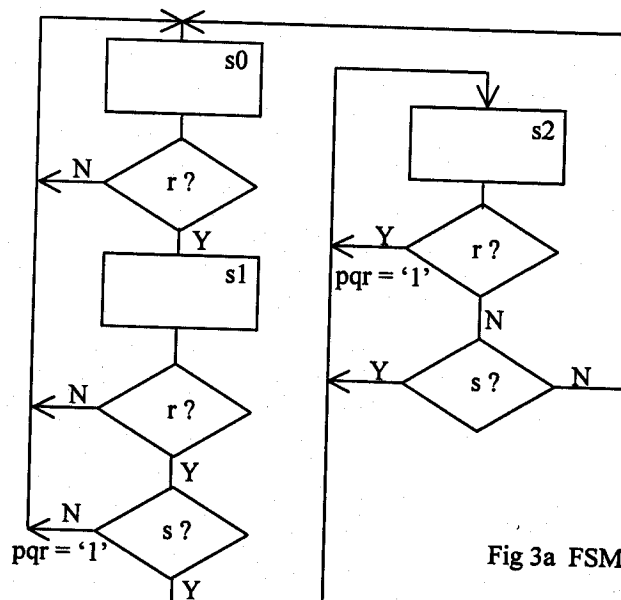


Fig 3a FSM Flow chart

FSM Flow Chart Key :

States : s0, s1, s2

signal name

Inputs : clk, rst, r, s

Output : pqr (unlatched o/p,
default value = '0')

- b) Explain with illustrations what is meant by the following

Concurrent VHDL

Sequential VHDL

(4 marks)

- c) Describe the circuit of fig 4(a) using structural VHDL architecture. Assume that VHDL models are already available for the counter and de-multiplexer. Use signal names provided in figure 3c

(5 marks)

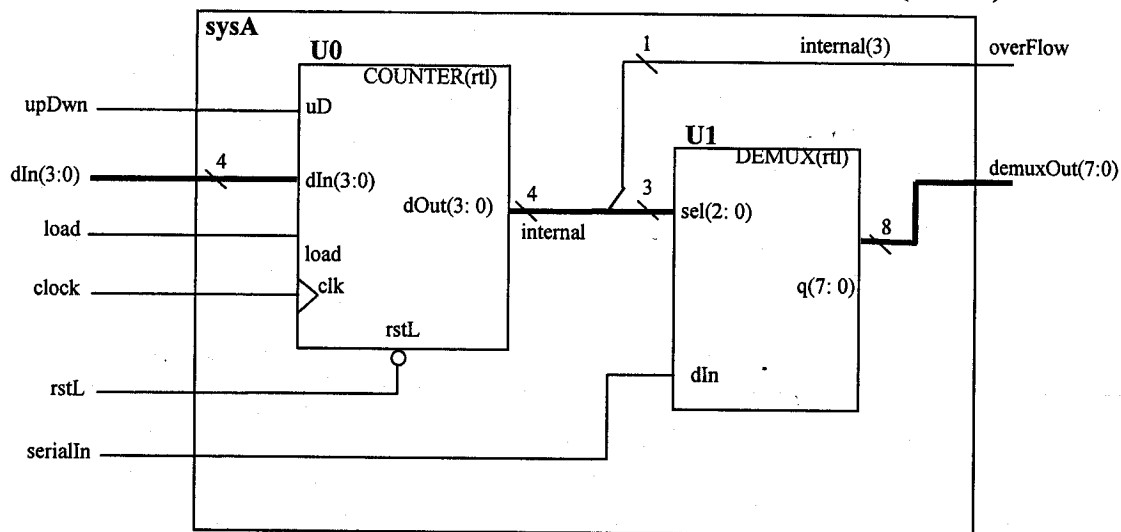


Figure 3c

- d) A 4-to-1 multiplexer has data output muxOut, data inputs A, B, C, D and control input SEL(1:0). MuxOut is selected using SEL(1:0) as follows : A (00), B(01), C(10), D(11). Assuming that data path C (SEL = "10") has a critical timing, write a VHDL model to provide a synthesised circuit with optimal timing performance.

(4 marks)

4. a) Create a VHDL model describing a sixty minute timer unit with symbol illustrated in fig 4(a)

(11 marks)

The timer counts from 00min:00sec to 59min:59sec

Assume that the following are provided :

System clock (clk) : frequency = 500kHz

Asynchronous reset signal (rst)

Synchronous one second input pulse signal, oneSec (assertion duration = 2us)

Use std_logic and std_logic_vector types throughout.

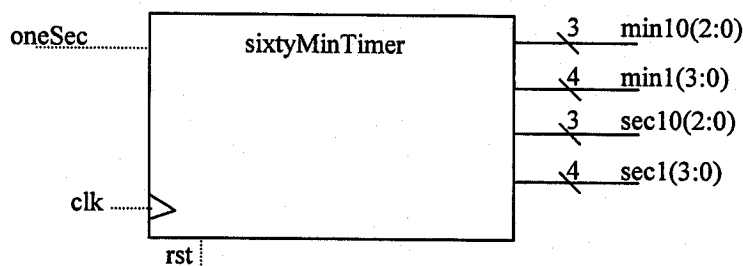


Figure 4(a) : sixty minute timer unit symbol

- b) Indicate the change to the VHDL model to provide synchronous load functionality (using an additional signal 'load')
- (3 marks)
- c) Compare the use of CASE and IF-THEN-ELSE blocks on synthesised circuit structure and performance.
- (2 marks)

- List the main features of this element and explain how combinational and sequential logic can be implemented in a CLB (4 marks)



Figure 4b Xilinx XC4K FPGA Configurable Logic Block (CLB) Architecture