GX555

OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER II (SPRING) EXAMINATIONS, 2000/2001

THIRD YEAR ELECTRONIC ENGINEERING
THIRD YEAR ELECTRONIC & COMPUTER ENGINEERING

SEMICONDUCTOR TECHNOLOGY (EE315)

Professor L.E. Davis
Professor D.J. Wilcox
Dr. F. Morgan

Duration of Examination : **2 hours**

Instructions: Answer **THREE** questions.
All questions carry equal marks.

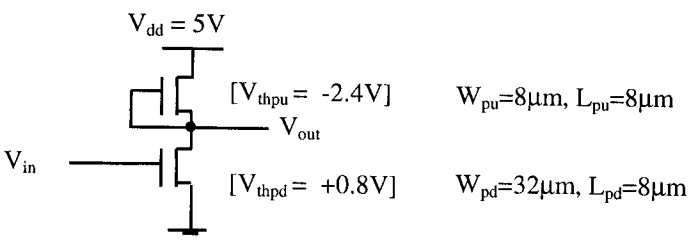
$$I_{ds}(lin) = \mu.C_{ox}\frac{W}{L}\left[\left(V_{gs}-V_{th}\right)V_{ds}-\frac{1}{2}{V_{ds}}^2\right] \qquad I_{ds}(sat) = \mu.C_{ox}\frac{W}{2L}\left(V_{gs}-V_{th}\right)^2$$

1. For the nMOS inverter of figure 1, calculate the following (clearly state and verify transistor operation modes in each case) :

a) the inverter output 'low' voltage (6 marks)

b) the current through each transistor in steady state when (3 marks)
   i) output is low
   ii) output is high

c) the input voltage to cause inverter output voltage (V_{out}) = 3.7V (4 marks)



$\mu C_{ox} = 20\mu A/V^2$

Figure 1

d) the inverter switching voltage (V_{inv}), assuming that both transistors operate in saturation at the inversion point. (3 marks)

e) the current flowing at the inverter switching point. (2 marks)

f) Illustrate (with a sketch) the effect of decreasing the Z_{pu}/Z_{pd} ratio on the inverter characteristic. (2 marks)

2. a) Briefly outline the typical nMOS fabrication process steps. Illustrate with a detailed sketch. (3 marks)

b) Explain why an nMOS transistor is used as the pulldown device in a CMOS inverter while a pMOS transistor is used as the pullup device. (5 marks)

c) Illustrate how CMOS technology offers improvements over nMOS-only technology (2 marks)

d) Calculate the CMOS inverter switching voltage (V_{inv}) for the following CMOS inverter transistor parameters : $V_{thpd}=-V_{thpu}=1V$, $W_{pd}/L_{pd}=2$, $W_{pu}/L_{pu}=4$, $\mu_n=2\mu_p$, $V_{dd}=5V$
Clearly state (and verify) transistor operation modes (4 marks)

e) Illustrate the advantage that can be gained by implementing a CMOS logic circuit using NAND gates rather than NOR gates (3 marks)

f) Highlight and comment on five aspects of MOS technology scaling. (3 marks)

3. a) Design a CMOS combinational logic circuit to implement the following function:

$$F = A.\overline{B} + C.D.(B + \overline{C})$$ Do not attempt any minimisation. (3 marks)
Indicate the required modifications to your CMOS logic circuit to convert it to an nMOS implementation (do not re-draw the circuit). (1 mark)

b) Draw the equivalent coloured mask stick diagram for the CMOS mask layout of figure 3 (provided on separate page) [Input signals : A, B, C. Output signal F] (4 marks)

c) Draw the MOS transistor level circuit diagram for the implementation of figure 3 and derive the boolean description for the circuit (5 marks)

d) Sketch the device layer profile for the section through the line L---L in figure 3.
Label all regions (e.g., silicon type, SiO_2 (gate & field), polysilicon gate, metal etc). (3 marks)

e) Sketch and explain the basic operation and application of a conventional BiCMOS inverter circuit. List typical BiCMOS applications. (4 marks)

4. a) Describe the operation of a CMOS transmission gate and comment on how it is superior to nMOS and pMOS pass transistors. (4 marks)

b) Illustrate an EXCLUSIVE-OR function implemented using transmission gates. Include a detailed truth table to illustrate the precise operation of the circuit. (4 marks)
Compare the number of transistors required to implement the EX-OR gate using
i. transmission gates
ii. CMOS gates (3 marks)

c) Illustrate a full adder functions implemented using transmission gates. (5 marks)

d) Describe latchup in BiCMOS circuits. Outline two methods used to minimise the occurrence of latchup (4 marks)