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OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER II EXAMINATIONS 2000/2001

THIRD YEAR ELECTRONIC ENGINEERING
THIRD YEAR ELECTRONIC AND COMPUTER ENGINEERING

EE321 ANALOGUE SYSTEMS DESIGN II

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Duration of Examination: **TWO** hours
Instructions: Answer **THREE** questions

1.

(a) Draw a simple model for the real diode. **[1 mark]**

(b) What is the purpose of the circuit in Fig. 1? **[2 marks]**

(c) For a sinusoidal input waveform V_S with a peak-to-peak voltage of 5 V, sketch the output waveform V_O if the characteristic curve of the real diode is as shown in Fig. 2. **[4 marks]**

(d) Describe the effect on V_O of placing a capacitor C in parallel with the load, i.e. between points A and B in the circuit. **[4 marks]**

(e) Give an expression for the percentage ripple on the output signal V_O when the capacitor is included in the circuit. **[4 marks]**

(f) Calculate the percentage ripple if the circuit parameters are as follows: the period of the input sinusoidal waveform is 16.7 ms, the input peak-to-peak voltage is 5 V, the load resistance is 100 Ω, and the capacitor value is 1000 μF. What would happen if C were increased? **[5 marks]**

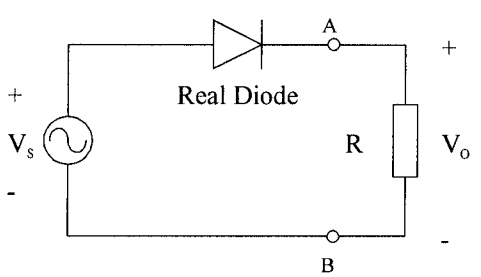

Fig. 1

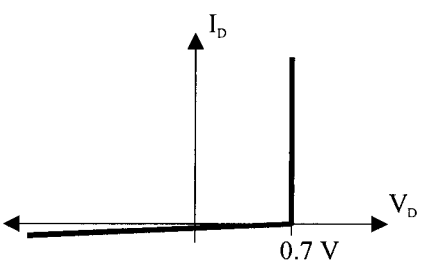

Fig. 2

[cont'd]

2.

(a) Write a short description for any three of the following types of diode. **[3 x 3 marks]**

- Schottky diode
- Varactor diode
- LED
- Flyback diode
- Photo diode

(b) A Zener diode circuit for voltage regulation is given in Fig. 3.

(i) Sketch the i_D vs. v_D characteristic for a Zener diode showing the various regions of operation. **[2 marks]**

(ii) In which region does the Zener diode operate for the voltage regulator application shown? **[1 mark]**

(iii) For varying source voltage and load current, analyse the circuit in Fig. 3 to determine the proper range of values for R_i that will allow the diode to maintain a constant output voltage (by keeping the Zener current between its minimum and maximum values). **[6 marks]**

(iv) Define percentage regulation for the Zener diode voltage regulator. **[2 marks]**

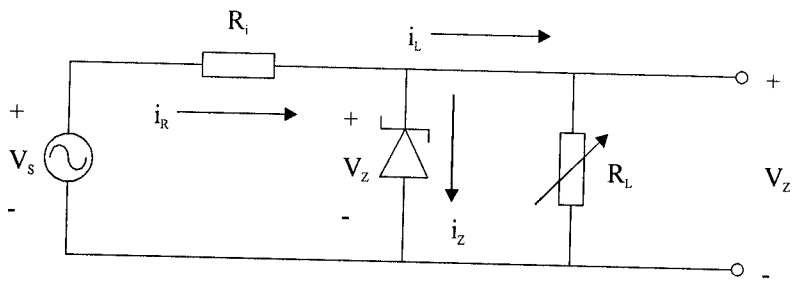

Fig. 3

3.

(a) What is meant by the term "common emitter"? **[1 mark]**

(b) Perform a DC analysis of the base biasing section of the common emitter amplifier as shown in Fig. 4, and hence derive formulæ for the position of the DC operating point. **[8 marks]**

(c) Calculate the DC operating point for this common emitter amplifier circuit with the component values given in Table 1. **[6 marks]**

(d) Find the value of I_B, i.e. the i_B characteristic on which the DC operating point lies. **[2 marks]**

(e) What is the equation of the DC load line for this common emitter amplifier circuit? **[3 marks]**

V_{CC} = 30 V	R_E = 2.2 kΩ
R_{B1} = 33 kΩ	R_C = 10 kΩ
R_{B2} = 4.7 kΩ	BJT β = 75

Table 1

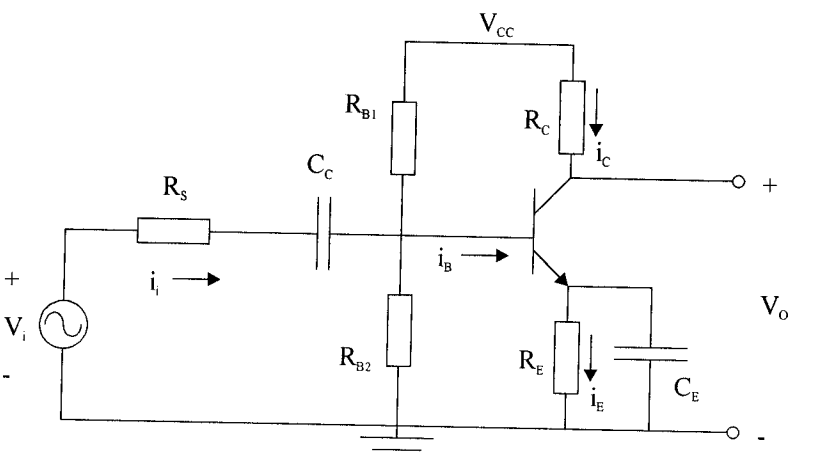

Fig. 4

[cont'd]

4.

(a) Sketch the physical structure of a Junction Field Effect Transistor (JFET). **[6 marks]**

(b) Draw the electrical circuit symbol for a JFET, labelling the terminals and showing the relevant currents and voltages. **[3 marks]**

(c) Why are two voltage supplies required for a JFET to operate? **[1 mark]**

(d) Sketch the states of JFET operation on an i_{DS} vs. v_{DS} characteristic. **[2 marks]**

(e) Give equations for (i) the voltage at which JFET pinch-off begins and (ii) the current in the pinch-off region. **[4 marks]**

(f) Sketch the i_{DS} vs. v_{DS} JFET characteristics for v_{GS} = 0, -1, -2 and -2.5 V with the specifications given below. **[4 marks]**

- I_{DSS} = 20 mA
- V_{GSCO} = -3V

5.

(a)

Explain the operation of an integrator using the following points in your explanation:

(i) Circuit diagram. **[2 marks]**

(ii) Derive an expression for v_o. **[6 marks]**

(iii) Sketch the v_o you would expect for a square wave input (your diagram should include both input and output waveforms). **[4 marks]**

(b)

Explain briefly what is meant by the following specifications in practical operational amplifier circuits (suggest typical values where appropriate).

(i) Input offset voltage. **[2 marks]**

(ii) Slew rate. **[2 marks]**

(c) Calculate the input offset voltage for the circuit in Fig. 5 given V_O = -8 V. **[4 marks]**

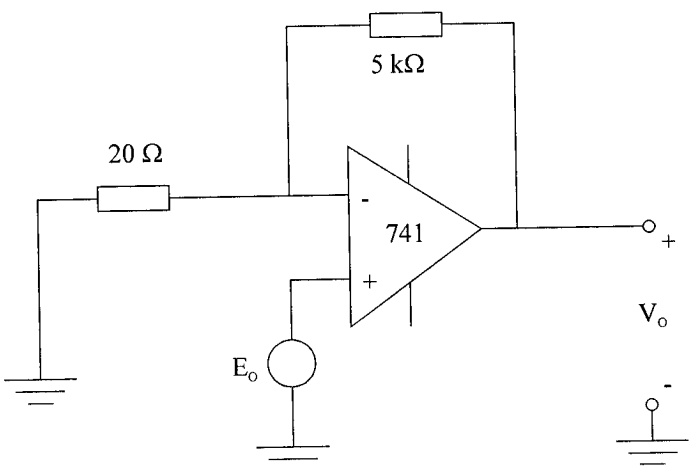

Fig. 5