GX560

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS, 2001

SECOND ELECTRONIC ENGINEERING
SECOND ELECTRONIC AND COMPUTER ENGINEERING

ANALOGUE SYSTEMS DESIGN I

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Duration of examination: *Two* hours

Instructions: Answer *four* questions

1 (a) (i) List and explain briefly the characteristics of an ideal operational amplifier. [4 marks]

(ii) Describe four properties of a real op-amp which highlight how it differs from the ideal. [4 marks]

(b) You are required to design a basic digital to analogue converter based upon an inverting operational amplifier configuration. A block diagram of the system is shown in Figure 1. The converter is to have four binary inputs which will have values of 0V or 5V only. The circuit is to give an output voltage equal in magnitude to the decimal value of the binary number applied at the input. The output voltage will be negative. Give a full circuit diagram for the DAC design and calculate the output voltages for all possible input binary combinations.

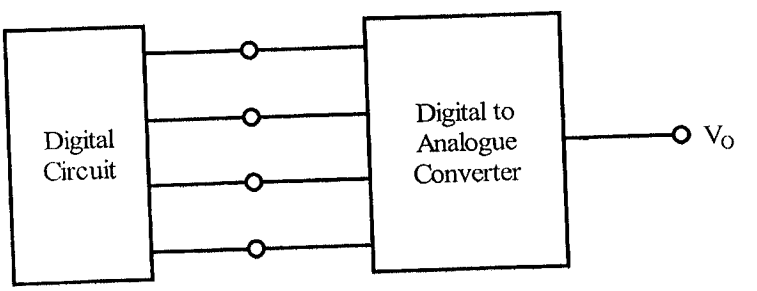


Figure 1

Specify the output resistance of your circuit and calculate the maximum current that the digital circuit would have to supply to the DAC. [17 marks]

2 **(a)** The diagram of Figure 2.1 below shows the general block diagram of a negative feedback amplifier. Derive an expression for the output voltage of the amplifier in terms of the input voltage V_i, forward gain A and feedback factor B. Proceed to show that for a real amplifier with limited supply voltage rails (+15V and -15V) the value of the voltage V_x is approximately zero. What implication does this result have for an inverting operational amplifier circuit.

[9 marks]

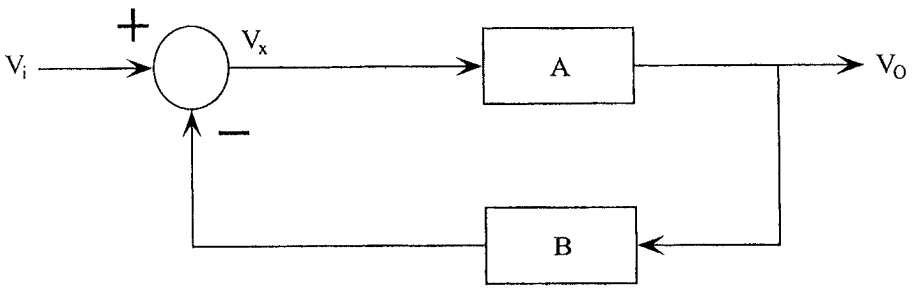


Figure 2.1

(b) **(i)** Assuming $R_1 = R_2$, determine an expression for the output voltage of the circuit of Figure 2.2.

[9 marks]

(ii) Using values of $R_1 = R_2 = 2k\Omega$ and $R_F = 10k\Omega$, plot cycles of the output if the following inputs are applied:

$$V_1(t) = 2V \text{ (DC) and}$$
$$V_2(t) = 0.1 \sin(2\pi 50t)$$

[7 marks]

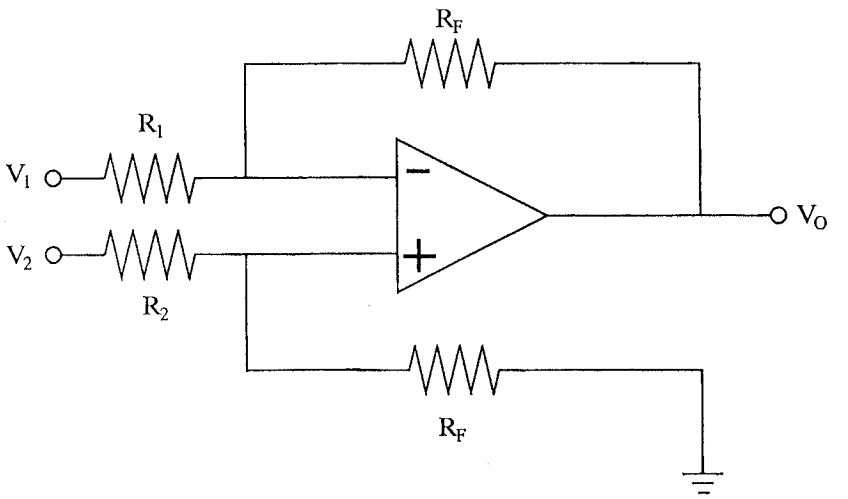


Figure 2.2

3 (a) Draw a diagram showing the semiconductor make up of an n-channel Junction Field Effect Transistor (JFET). Explain how the phenomenon known as *Pinch-Off* occurs in a JFET. Define the *pinch-off voltage* of a JFET.

[6 marks]

(b) For the circuit of figure 3 below calculate the gate, source and drain voltages and specify clearly the drain current flowing.

[19 marks]

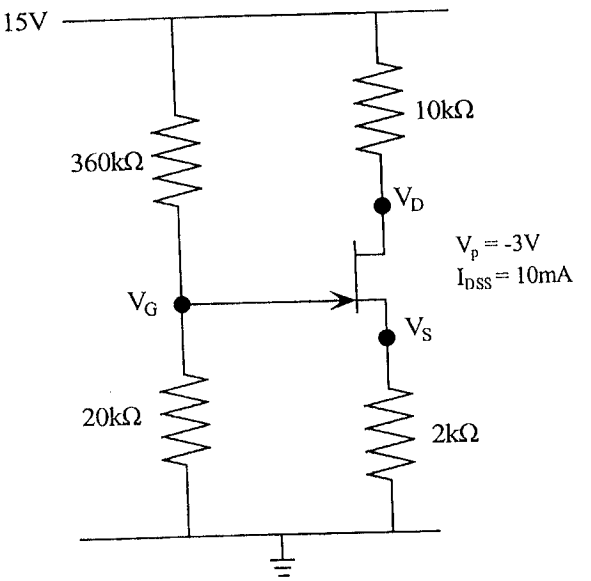


Figure 3

4 (a) Draw a diagram showing the semiconductor make up of an n-channel, depletion mode metal oxide field effect transistor (MOSFET). Sketch the I-V curves for such a device. Explain the difference between the depletion and enhancement modes of operation of a MOSFET.

[6 marks]

(b) Determine the DC bias levels of the transistor in the circuit of figure 4 below.

[19 marks]

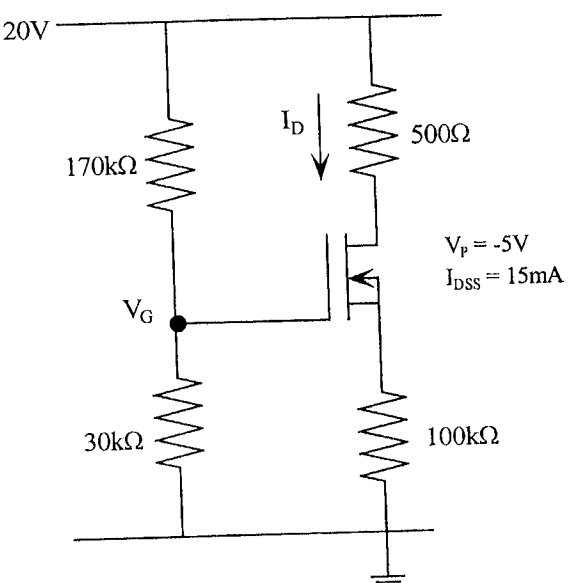


Figure 4

5 **(a)** Explain briefly the purpose of biasing a transistor amplifier circuit. Proceed to calculate the DC bias levels of V_B, V_C, V_E, I_B, I_E and I_C of the circuit of figure 5 below.

[10 marks]

(b) Calculate the voltage gain of the circuit.

[10 marks]

(c) If the input voltage v(t) is a sinusoid voltage of peak value V_p=10mV sketch the output voltage waveform over two cycles.

[5 marks]

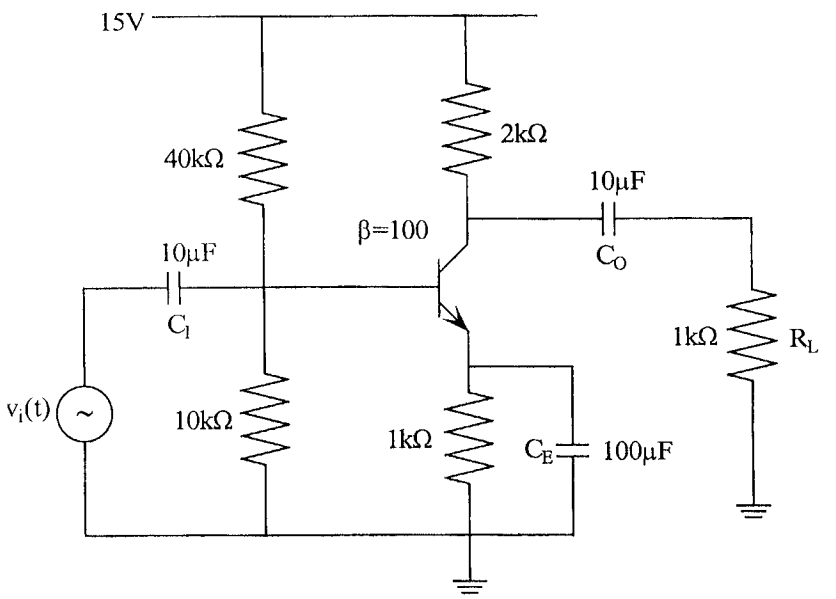
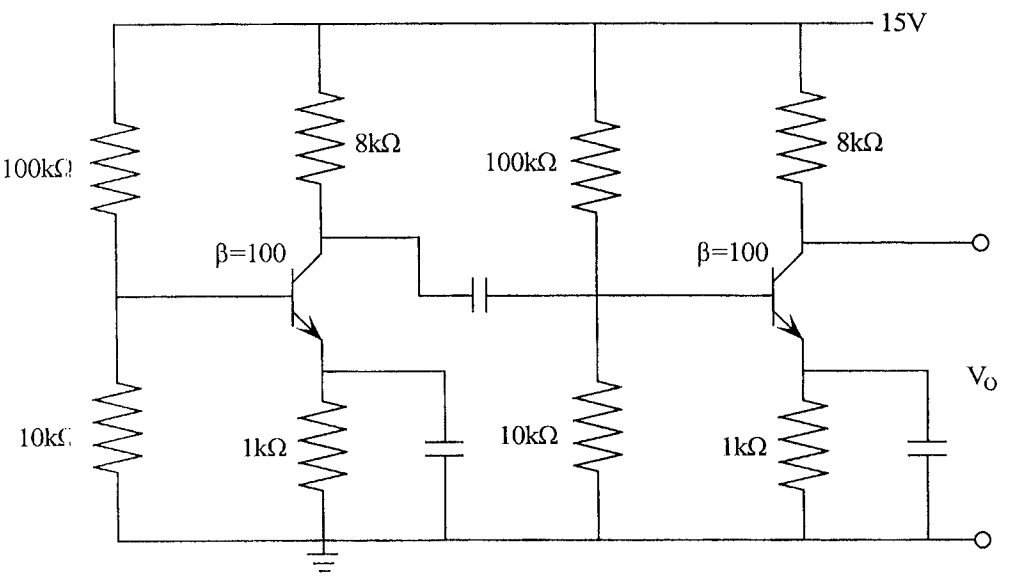


Figure 5

6 **(a)** Determine an equivalent circuit model of the multistage common-emitter transistor circuit of figure 6 below. Specify clearly the voltage gain of the circuit.

[20 marks]



(b) If a microphone of output resistance R_O = 100Ω producing a output signal of 1mV peak voltage is connected to the amplifier, predict the peak value of the output.

[5 marks]