GX564

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NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER II EXAMINATION, 2000/2001

4TH YEAR ELECTRONIC & COMPUTER ENGINEERING

EMBEDDED SYSTEMS

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Duration of Examination: *Two* hours

Instructions: Section A - Answer **all** questions
Section B - Answer **two** questions

Section A

Attempt all questions in this section – 40 marks; 2 marks per question.
(NB: where applicable you must include rough-work calculations to obtain full marks for these questions.)

A1. Why is the Harvard architecture potentially faster than the von Neumann? Because Harvard CPUs,

(a) have faster clocks (b) use fewer clock cycles (c) have two memory buses
(d) has RISC architecture (e) have one memory bus (e) none of the above

A2. What functions are in a microcontroller chip but NOT in a microprocessor?

(a) Interrupts (b) Instruction Decoder, Instruction Register
(c) Program Memory, Data Memory, I/O (d) Program Counter, Registers, Data Bus
(e) Peripherals, Address & Data Buses (f) none of the above

A3. From what point of reference are the terms "read" and "write" defined.

(a) The CPU (b) The I/O Device (c) The Data Bus
(d) The Address Bus (e) The Memory (f) none of the above

A4. How many address spaces does the 8051 family of CPUs have?

(a) 1 (b) 2 (c) 3
(d) 4 (e) 5 (f) none of the above

A5. How does the 8051 CPU indicate when it is fetching an instruction from external program memory? It activates the,

(a) /RD signal (b) XTAL signal (c) ALE signal
(d) /PSEN signal (e) /RESET signal (f) none of the above

A6. How does the 8051 CPU indicate when it is reading external data memory? It activates the,

(a) /RD signal (b) XTAL signal (c) ALE signal
(d) /PSEN signal (e) /WR signal (f) none of the above

A7. How does the 8051 CPU indicate when it is writing to internal data memory? It activates the,

(a) /RD signal (b) XTAL signal (c) ALE signal
(d) /PSEN signal (e) /WR signal (f) none of the above

A8. If a logic output has I_{OL} = 10 mA and I_{IL} = 2 mA what is the logic zero fanout?

(a) fanout = 2 (b) fanout = 5 (c) fanout = 10
(d) fanout = 15 (e) fanout = 20 (f) none of the above

A9. If a logic output is specified for operation with a maximum load, C_L = 100 pF and the input capacitance of the logic family is 15 pF what is the maximum AC fanout?

(a) 6 (b) 7 (c) 8
(d) 10 (e) 15 (f) none of the above

A10. What restrictions are imposed when erasing/writing to Flash EPROM? Data is,

(a) always written on word boundaries
(b) written/erased only one byte at a time
(c) erased in complete sectors/blocks
(d) only erasable with UV strobe light
(e) only writable one time
(f) none of the above

A11. How can you erase a UV Eprom non-destructively?

(a) by voltage reversal
(b) by shining a black light on it
(c) by heating to 50°C
(d) by positron irradiation
(e) by X-Ray irradiation
(f) none of the above

A12. What is the maximum number of bits that can be stored in a byte-wide ROM in a 32 pin package?

(a) 128 K x 8 = 1 Mb
(b) 1 M x 8 = 8 Mb
(c) 2 M x 8 = 16 Mb
(d) 4 M x 8 = 32 Mb
(e) 8 M x 8 = 64 Mb
(f) none of the above

A13. For a DRAM what is the largest memory that can be packaged in a 24 pin package?

(a) 16 Mb
(b) 32 Mb
(c) 64 Mb
(d) 4 Gb
(e) 64 Gb
(f) none of the above

A14. What is the largest byte-wide SRAM that will fit into a 32 pin package?

(a) 256K x 8 = 2 Mb
(b) 512K x 8 = 4 Mb
(c) 1 M x 8 = 8 Mb
(d) 2 M x 8 = 16 Mb
(e) 4 M x 8 = 32 Mb
(f) none of the above

A15. A von Neumann architecture 8 bit CPU has 16 address lines. How much memory can it address?

(a) 256 B
(b) 64 kB
(c) 128 kB
(d) 4 MB
(e) 16 MB
(f) none of the above

A16. A Harvard architecture 8 bit CPU has 16 address lines. How much memory can it address?

(a) 256 B
(b) 64 kB
(c) 128 kB
(d) 256 kB
(e) 4 MB
(f) none of the above

A17. Which registers do PUSH and POP instructions operate on?

(a) SP only
(b) SP and TCON
(c) SP and SCON
(d) SP, IP and IE
(e) SP and int. memory
(f) none of the above

A18. What type of instructions are ANL, ORL and XRL?

(a) Arithmetic
(b) Data
(c) Boolean
(d) Logical
(e) Branch & Control
(f) none of the above

A19. What type of instructions are CJNE and RETI?

(a) Arithmetic
(b) Data
(c) Boolean
(d) Logical
(e) Branch & Control
(f) none of the above

A20. The data pointer register may be used to implement?

(a) the interrupt stack
(b) look-up tables
(c) the RS232 port
(d) system timers
(e) I/O functions
(f) none of the above

Section B

Attempt 2 questions in this section – 60 marks; 30 marks per question.
(NB: Candidates should note that marks may be lost if answers are not presented in a neat and orderly manner)

B 1. **(a)** Describe and sketch the layout of a root file system. List the data fields that would be required in a root file system with accompanying explanations where necessary.

[9 marks]

(b) List five functions that a real-time executive performs and describe each in brief.

[9 marks]

(b) Explain the differences between: (i) cooperative and pre-emptive switching; (ii) inter-process and inter-processor communications (iii) processes and threads and (iv) file and process control blocks.

[12 marks]

B 2. **(a)** Sketch a block diagram of the 8051 chip. Explain, briefly the function of each peripheral or subsystem of the 8051. Sketch a memory map describing the organization of the internal memory of the 8051.

[12 marks]

(b) Write short 8051 assembly language segments to implement the following operations

(i) X1 := Y + 7 (ii) X1 := Y + Z
(iii) X1 := Y - Z - 3 – T (iv) IF X1 < 10 then Y := Z * 2
(v) IF X1 = 2 THEN Y := Y + 4 ELSE Z := 0

[18 marks]

B 3. **(a)** Explain, using short segments of assembly language how the parallel I/O ports of an 8051 can be used to perform (i) byte transfer and (ii) bit manipulation.

[6 marks]

(b) Describe the operation of the 8051 serial port. Explain how it can be initialised for use in software-polled mode. Provide short segments of assembly language to implement (i) polled initialisation, (ii) polled receive and (iii) polled transmit.

[12 marks]

(c) Explain how interrupts work. How could you modify the serial port routines under part (b) to work with interrupts? Provide assembly code implementations of these routines.

[12 marks]

B 4. **(a)** Describe the principle differences between a *microprocessor* and a *microcontroller*. List and describe four peripherals commonly found on 8-bit microcontrollers.

[9 marks]

(b) How could the following embedded code segments be rewritten to be more efficient?

(i)
```
x**2;
```

(ii)
```
a = (b+c) * f ;
d = g * (b+c);
```

(iii)
```
for (I = 0; I < N ; I++) {
    b = k * t;
    a[I] = j * (b+c);}
```

[9 marks]

(c) Describe the main steps in developing a new embedded product. As a practical example describe, in overview, the hardware and software design of a portable MP3 player indicating the various factors which can influence final design for such a product.

[12 marks]

B 5. **(a)** There are 4 addressing modes available on the 8051 CPU. List and describe them, giving short assembly code listings and sketching diagrams to illustrate the differences between addressing modes.

[9 marks]

(b) How many low-power Schottky TTL loads can a CMOS gate drive? How many additional CMOS gates can be added to the maximum number of TTL gates?

*(Use the device parameters given in **Table No. 1** and **Table No. 2** in the Appendix.)*

[12 marks]

(c) Sketch logic voltage levels – both input and output – for CMOS and TTL gates. Explain why TTL cannot drive CMOS reliably. Suggest a circuit modification to overcome this limitation of TTL devices.

[9 marks]
