GX2644

OLLSCOIL NA hEIREANN
THE NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER 2 EXAMINATIONS 2000-2001

MASTERS IN SOFTWARE DESIGN AND DEVELOPMENT

CT516 COMPUTER ARCHITECTURE AND OPERATING SYSTEMS

Professor D. Bell
Professor G. Lyons
Mr. A. Reilly

Time allowed: THREE hours
Answer 5 questions. All questions carry equal marks
At least two questions must be answered from each section.
Please use a separate answer book for each section

SECTION A

Q1. (a) (i) Distinguish between computer architecture and computer organisation. (3)
(ii) Describe briefly the functional view of a computer system. (6)

(b) Describe and sketch a typical high-performance bus architecture and distinguish it from a traditional bus architecture. (6)

(c) Describe briefly the basic (no interrupts) instruction cycle. (5)

Q2. Describe briefly, using diagrams where appropriate, any 3 of the following (20)

(a) CPU Addressing Modes

(b) Instruction Pipelining

(c) Cache Memory

(d) Hard Disk Drives

Q3. (a) (i) Describe the operation of Direct Memory Access (DMA). (6)
(ii) Compare and contrast the P1394 Firewire and Universal Serial Bus (USB) external interfaces. (4)

(b) Perform the following arithmetic in binary using two's compliment: (4)
(i) -2 +7
(ii) 4- 3

(c) Calculate the 32 bit floating-point representation of 1.31072×10^6. (6)

Q4. (a) Distinguish between *sequential* and *combinational* circuits, outlining where sequential circuits might be used. (4)

(b) Use logic diagrams and truth tables to express the following Boolean relationships and determine the single gate equivalent circuit: (10)

(i) $\overline{(\overline{A} \text{ OR } B) \text{ AND } (A \text{ XOR } \overline{B})}$

(ii) $\overline{(\overline{A} \text{ AND } \overline{B}) \text{ OR } (A \text{ XOR } B)}$

(b) Describe the operation of the half adder. Indicate how it can be expanded to perform full addition. (6)

SECTION B

Q5. (a) Describe, with the aid of a block diagram, the Process Control Block. (8)

(b) (i) Outline the events in an OS that can trigger a process switch. (6)
(ii) Describe the series of tasks that the OS must carry out in the event of a process switch. (6)

Q6. (a) Explain external fragmentation and how it occurs in a dynamic partitioning approach to memory management. (6)

(b) In a simple paging memory management scheme, describe with the aid of a diagram how a logical address of a page can be translated into a physical address. (8)

(c) Describe briefly the LRU and FIFO page replacement policies. (6)

Q7. Write notes on 3 of the following (20)

(a) Process Scheduling

(b) Disk Space Allocation Methods

(c) Viruses and other software threats

(d) Handling Deadlocks in an OS

(e) Middleware

Q8. (a) (i) What are the characteristics of a real-time operating system? (4)
(ii) Describe how real-time tasks can be scheduled based on starting and completion deadlines. (6)

(b) (i) Describe a generic client/server environment. (5)
(ii) Discuss database applications in the context of the client/server. (5)