Ollscoil na hÉireann, Gaillimh GX 685
National University of Ireland, Galway

Semester II Examinations (Spring), 2002/2003

Exam Code(s)	3BN121, 3BP121
Exam(s)	3rd Electronic Engineering 3rd Electronic & Computer Engineering
Module Code(s)	EE315
Module(s)	SEMICONDUCTOR TECHNOLOGY
Paper No.	1
Repeat Paper	Special Paper
External Examiner(s)	Professor S. Mc Laughlin
Internal Examiner(s)	Professor D.J. Wilcox Dr. F. Morgan Mr. S. Porter
Instructions:	Answer **THREE** questions. All question carry equal marks.
Duration	2 hrs
No. of Answer books	
Requirements:	
Handout	
MCQ	
Statistical Tables	
Graph Paper	
Log Graph Paper	
Other Material	
No. of Pages	
Department(s)	Electronic Engineering

Question 1

$$I_{ds}(lin) = \mu.C_{ox}\frac{W}{L}\left[\left(V_{gs}-V_{th}\right)V_{ds}-\frac{1}{2}V_{ds}{}^{2}\right] \qquad I_{ds}(sat) = \mu.C_{ox}\frac{W}{2L}\left(V_{gs}-V_{th}\right)^{2}$$

1.

For the nMOS inverter of Figure 1(a), calculate the following (clearly state and verify transistor operation modes in each case):

a) the inverter output 'low' voltage, V_{OL} (5 marks)

b) the inverter output 'high' voltage, V_{OH} (2 marks)

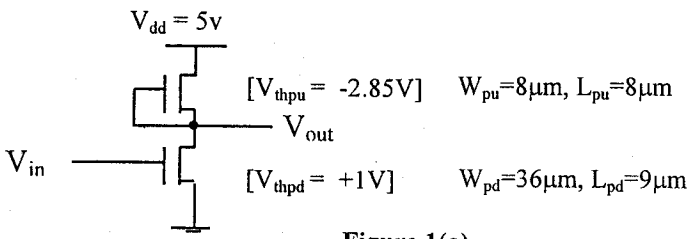


Figure 1(a)

c) The Voltage Transfer Characteristic of the Inverter above is shown in Figure 1(b), deduce V_{IL}, V_{IH} and hence calculate NM_L and NM_H. (3 marks)

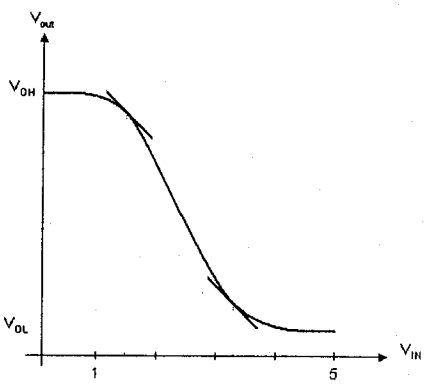


Figure 1(b)

d) Determine the Dynamic Power Dissipation for the Inverter when operated at a frequency F =1MHz with Load Capacitance CL = 1pF. (2 marks)

e) Briefly describe the operation of both a depletion and enhancement mode device and draw ID/VGS characteristics for both devices. (3 marks)

f) The early nmos Inverter used a fixed resistive load for the pull up device. Discuss the problem with using this approach and the subsequent problems associated with the two most common methods used to create this resistance. (3 marks)

g) Define the terms fan-in and fan-out. (2 marks)

Question 2

2.

a) State how the CMOS inverter offers improvements over nMOS-only technology. (2 marks)

b) Calculate the CMOS inverter switching voltage (V_{inv}) for the following CMOS inverter transistor parameters: $V_{thpd} = +1V$, $V_{thpu}=-1V$, $W_{pd}/L_{pd}=2$, $W_{pu}/L_{pu}=4$, $\mu_n=2\mu_p$, $Vdd=5V$
Clearly state (and verify) transistor operation modes. (5 marks)

c) Calculate the CMOS inverter current at the inverter switching point.
$K_{pd}=\mu C_{ox} = 20\mu A/V^2$ (2 marks)

d) State the Miller effect and hence use it to convert the circuit in Figure 2(a) to its Miller equivalent. (2 marks)

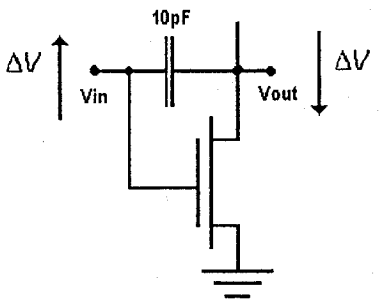


Figure 2a

e) State practical considerations that should be implemented when dealing with CMOS IC's. (2 marks)

f) Sketch and label a 2D structure of the CMOS P-Well device. (4 marks)

g) State the two advanced technologies used for CMOS fabrication and the benefits of each technology over standard P & N Well technologies. (3 marks)

Question 3

3.

a) Design a CMOS combinational logic circuit to implement the following function:

$$F = (A + B).(C + D).E$$ (4 marks)

Do not attempt any minimisation.

b) Draw the equivalent circuit diagram and coloured mask stick diagram for the CMOS circuit described by the Boolean equation

$$F = \overline{A.B+C}$$ (4 marks)

Do not attempt any minimisation.

c) Comment on four aspects of MOS technology scaling. (2 marks)

d) Design a Three State (H,L,Z) CMOS buffer. (2 marks)

e) Illustrate the advantage that can be gained by implementing a CMOS logic circuit using NAND gates rather than NOR gates. (2 marks)

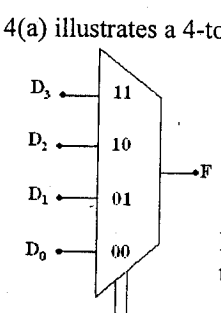
f) Sketch and explain the basic operation of a conventional BiCMOS inverter circuit. (3 marks)

g) Discuss effects that can trigger Latchup and possible prevention and suppression techniques. (3 marks)

Question 4

4.

a) Figure 4(a) illustrates a 4-to-1 multiplexer symbol.



Design a transmission gate circuit to implement this multiplexer function. Label all signals.

Figure 4a (5 marks)

b) Convert the static circuit shown in Figure 4(b) to its dynamic equivalent and state the advantages of dynamic logic design. (3 marks)

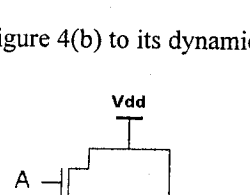


Figure 4b

c) State a solution to the problem of charge leakage in dynamic circuits and modify the circuit designed in (b) to reflect this. (1 marks)

d) Explain the problem of cascading dynamic gates and how domino logic deals with this issue. (3 marks)

e) Discuss SRAM and DRAM. (2 marks)

f) Design the ROM of Figure 4(c) to implement the truth table shown in Figure 4(d). (3 marks)

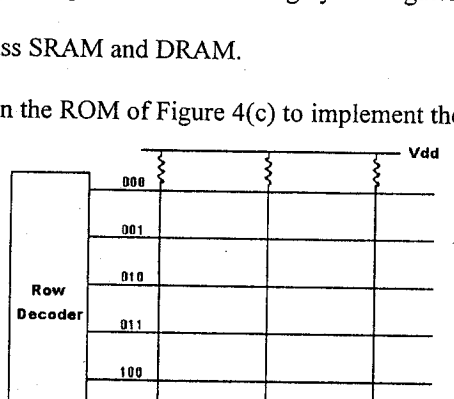


Figure 4c

a	b	c	f1	f2	f3
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0

Figure 4d

g) Discuss Latch vs Flip Flop with the aid of a timing diagram. (3 marks)