GX687

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SEMESTER II EXAMINATIONS 2002/2003

THIRD YEAR ELECTRONIC ENGINEERING
THIRD YEAR ELECTRONIC AND COMPUTER ENGINEERING

EE321 ANALOGUE SYSTEMS DESIGN II

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Duration of Examination: **TWO** hours
Instructions: Answer **THREE** questions

1.

(a) For the half-wave rectifier circuit with a real diode as shown in Fig. 1 (a):

(i) Sketch the output waveform V_o without the capacitor C in the circuit **[2 marks]**.
(ii) Describe the effect on V_o of placing the capacitor C in parallel with the load, i.e. between points A and B in the circuit **[3 marks]**.
(iii) Calculate the ripple voltage and percentage ripple if C is included **[4 marks]**.

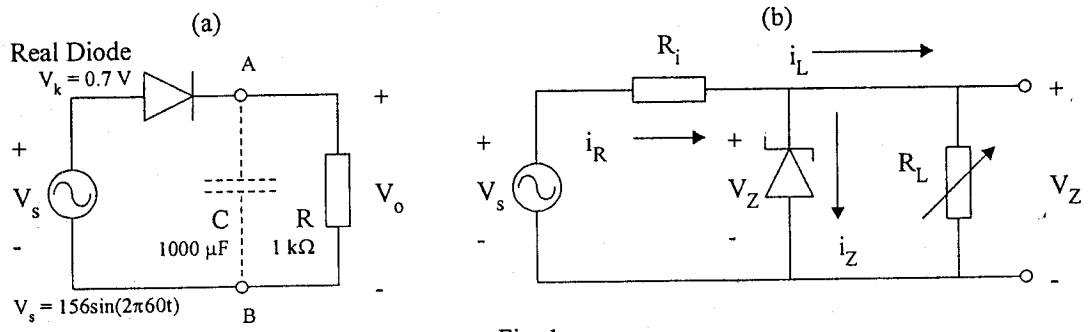

Fig. 1

(b) For the Zener diode voltage regulator circuit given in Fig. 1 (b):

(i) Sketch the i_D vs. v_D characteristic for a Zener diode showing the various regions of operation **[2 marks]**.
(ii) In which region does the Zener diode operate for the voltage regulator application shown **[1 mark]**?
(iii) For varying source voltage and load current, analyse the circuit to determine the proper range of values for R_i that will allow the diode to maintain a constant output voltage (by keeping the Zener current between its minimum and maximum values) **[6 marks]**.
(iv) Define percentage regulation for the Zener diode voltage regulator **[2 marks]**.

[cont'd]

2.

(a) Perform a DC analysis of the base biasing section of the common emitter amplifier as shown in Fig. 2, and hence derive formulæ for the position of the DC operating point on the characteristic curves **[8 marks]**.

(b) Explain why it is important for small signal voltage amplification to set the quiescent point in the BJT's linear mode of operation using the DC bias circuit **[4 marks]**.

(c) What is the effect of the bypass capacitor C_E in this circuit **[1 mark]**?

(d) Draw a small signal model for the common emitter amplifier circuit in Fig. 2, and using this model derive an expression for the gain of the amplifier **[7 marks]**.

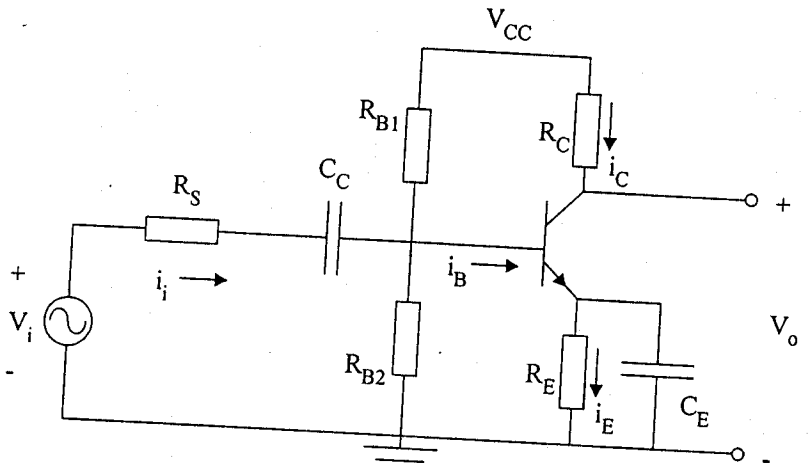

Fig. 2

3.

(a) Illustrate the operating modes of the n-channel JFET device using cross sectional diagrams **[6 marks]**.

(b) Calculate the DC operating point of the JFET amplifier shown in Fig. 3, where I_{DSS} = 8 mA and V_{DSPO} = 6 V **[9 marks]**.

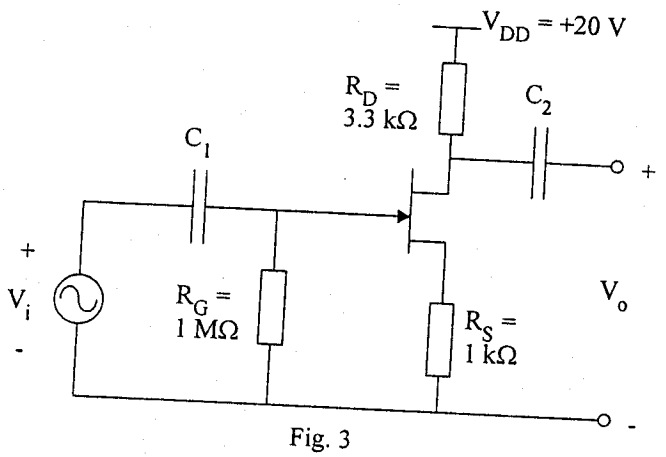

Fig. 3

(c) Illustrate with a cross-section a D-MOSFET and explain how the conducting channel can be "enhanced" by a correctly applied gate voltage **[5 marks]**.

[cont'd]

4.

(c) Explain the operation of an integrator using the following points in your explanation:
   (i) Circuit diagram **[3 marks]**.
   (ii) Derive an expression for v_o **[6 marks]**.
   (iii) Sketch the v_o you would expect for a square wave input (your diagram should include both input and output waveforms) **[4 marks]**.

(d) Explain briefly what is meant by the following specifications in practical operational amplifier circuits (suggest typical values where appropriate):
   (i) Input offset voltage **[2 marks]**.
   (ii) Slew rate **[2 marks]**.

(e) Calculate the input offset voltage for the circuit in Fig. 4 given $V_o = -8$ V **[3 marks]**.

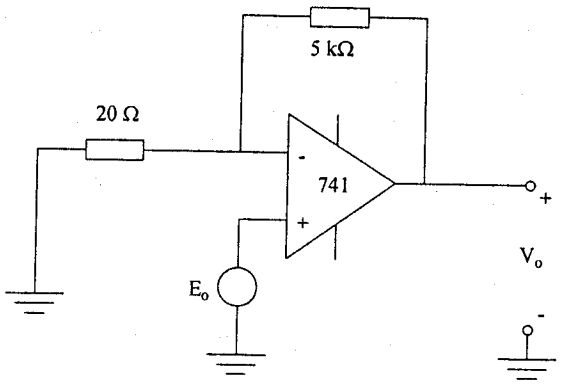

Fig. 4

5.

(a) An LC-tuned circuit has a capacitance of C = 0.47 pF. Find the inductance needed to produce oscillations with a frequency of f_o = 10 MHz **[3 marks]**.

(b) A Colpitts oscillator is designed to produce a resonant frequency of 100 MHz. If the inductor used is 0.1 mH, and we want a feedback factor of H = 0.2, calculate the required capacitor values C_1 and C_2 **[7 marks]**.

(c) Find V_{ref}, PW, T and f_o for the square wave generator of Fig. 5 (a) **[5 marks]**.

(d) For the 555 circuit as shown in Fig. 5 (b):
   (i) What are PW, T and f_o **[3 marks]**?
   (ii) Sketch the output voltage of the circuit **[2 marks]**.

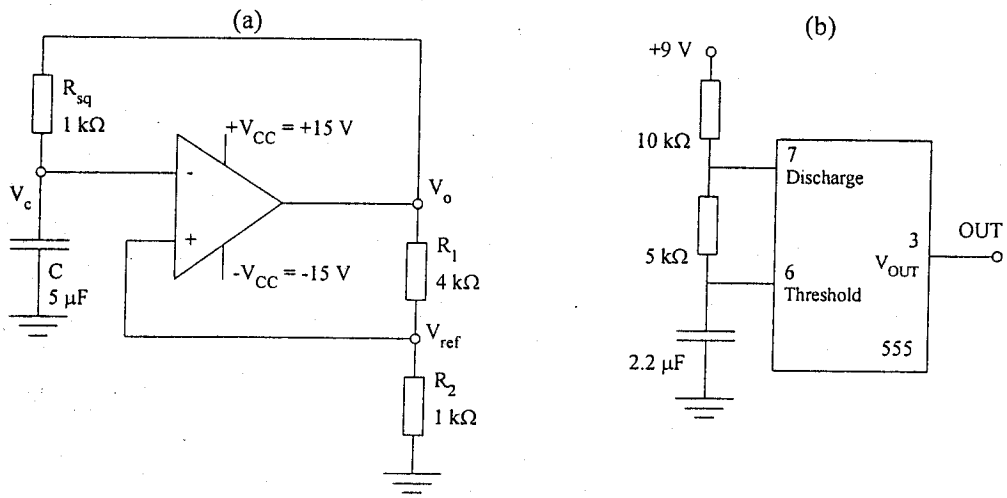

Fig. 5