Ollscoil na hÉireann, Gaillimh GX 694
National University of Ireland, Galway

Semester II Examinations, 2002/2003
Front Page Template

Exam Code(s)	4BN121, 4BP121
Exam(s)	MICROELECTRONICS AND VLSI DESIGN
Module Code(s)	EE419
Module(s)	
Paper No.	2
Repeat Paper	Special Paper
External Examiner(s)	Professor S. McLaughlin
Internal Examiner(s)	Professor D.J. Wilcox Dr. F. Morgan
Instructions:	Answer three questions All questions carry equal marks.
Duration	2 hrs
No. of Answer books	1
Requirements:	
Handout	1
MCQ	
Statistical Tables	
Graph Paper	
Log Graph Paper	
Other Material	
No. of Pages	5
Department(s)	Electronic Engineering

1. a) Define and explain the asynchronous feedback circuit fundamental mode restriction.(2 marks)

b) Explain the problem of metastability for asynchronous inputs to a synchronous system. Illustrate using circuit and timing diagrams. (3 marks)

c) Illustrate a commonly used circuit technique for minimising the risk of metastability on an asynchronous input to a synchronous system. On your circuit diagram, label and indicate the influence of each variable in the following MTBF equation. (3 marks)

$$MTBF = \frac{\exp\left(T \times [t_{clk} - t_{pd} - t_{setup}]\right)}{f_{clk} \times f_{in} \times T_0}$$

t_{clk} :	clk period
t_{pd} :	propagation delay through combinational logic between flip flops
t_{setup} :	flip flop setup time
f_{in} :	frequency of asynchronous i/p signal changes
T, T_0 :	experimentally derived *constants* for flip flop

d) What is the effect on MTBF of (2 marks)
i) increasing the synchronous system clock speed ?
ii) increasing the frequency of asynchronous i/p signal changes ?
Explain why.

e) Define, with illustration, the meaning of a static-1 hazard.
Consider the circuit of figure 1a. Explain whether any part of this circuit exhibits a hazard. If so, propose how the hazard may be removed. (6 marks)

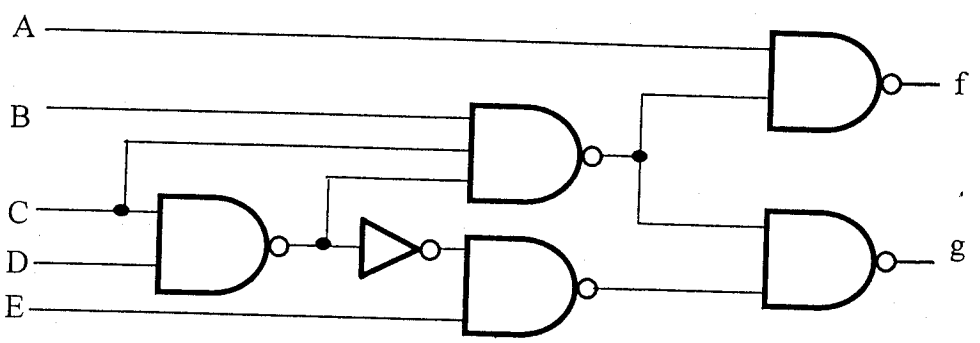

Fig 1a Asynchronous circuit

f) Define the difference between a D-Latch and a D-Flip flop. Illustrate using timing diagrams (1 mark)

g) Explain the operation of each part of the circuit test structure (figure 1b) and reason for its usage. (3 marks)

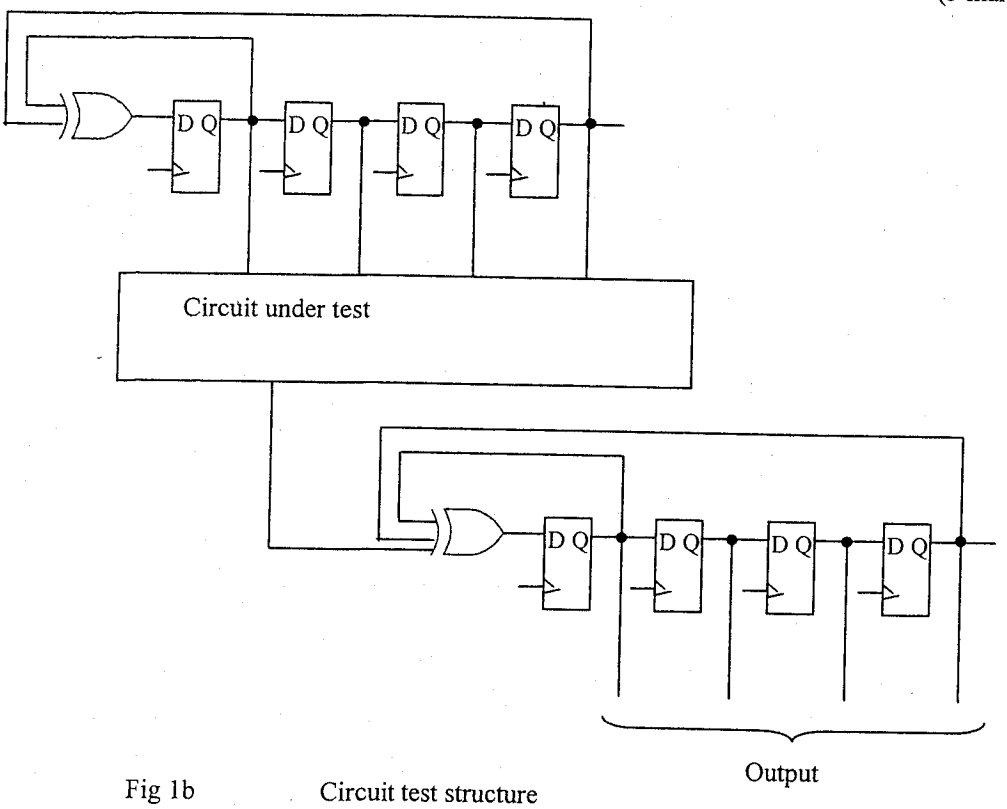

Fig 1b Circuit test structure

2. a) List and explain three potential benefits of using asynchronous design rather than the traditional synchronous design methodology. (2 marks)

b) Highlight and explain the existence of any RACE, CYCLE or undefined transition conditions in the asynchronous feedback circuit described by the excitation map (fig 2b) and block diagram (fig 2a). Explain how the excitation map of figure 2b could be modified to remove any unwanted or undefined transitions. (3 marks)
Assume state 10 is a dummy (unused) state where excitation map cell values may be modified to remove any unwanted transitions.

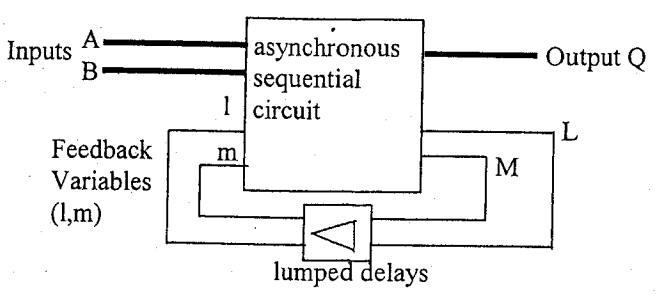

Fig 2a Asynchronous feedback circuit block diagram representation

lm	*AB* = 00	01	11	10	Output *Q*
	L M				
00	(00)	(00)	10	01	0
01	00	(01)	10	(01)	0
11	00	01	(11)	(11)	1
10	--	--	00	--	-

Fig 2b Asynchronous feedback circuit excitation map

c) Figure 2c illustrates an asynchronous sequential circuit

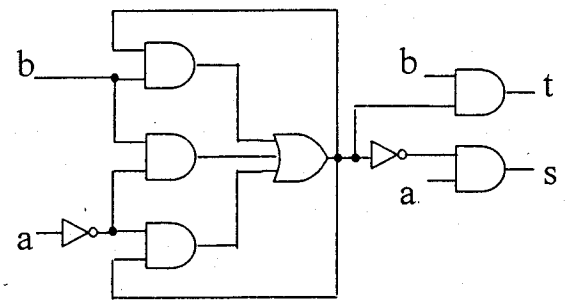

Figure 2c Asynchronous sequential circuit

Use a clear reverse engineering methodology to generate a minimal state diagram representing the functionality of the circuit. Include input & output signal values and state name on the state diagram and a key explaining the state diagram format. (7 marks)

d) Describe the difference between ASIC testing and ASIC verification. (4 marks)
Explain the ATPG process (preferably in flow chart form)

e) Explain boundary scan operation and its application (4 marks)

3. The timing diagram of figure 3 illustrates the behaviour of an asynchronous sequential system
Inputs : X_1 , X_2 Output : Z

Design an asynchronous sequential circuit to implement the system. (20 marks)
Generate boolean equations for all signals (you are not required to draw the circuit diagram).
Use a clear design & documentation methodology. Check and confirm that the design does not exhibit any race or hazard conditions (highlight and remove any, if detected).
Clearly state and explain any assumptions made.
Note : figure 3 is also included on separate sheet for submission with examination script.

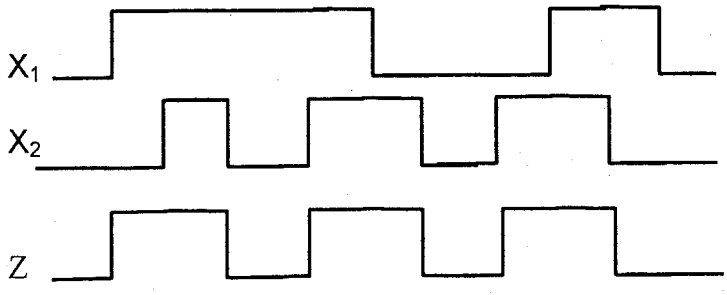

Figure 3 Timing diagram describing the behaviour of an asynchronous sequential system

4. a) Explain the following testability concepts (3 marks)
   i. Controllability
   ii. Observability

b) List four possible physical causes of a stuck-at fault in an ASIC. (2 marks)

c) A partially completed fault detection table for the combinational circuit of figure 4a is illustrated in fig 4b (see attached sheet at end of examination paper). Complete the fault detection table and derive a minimal test vector set for the circuit. (6 marks)
Submit figure 4b with your answer sheet. Include your detailed test set derivation work.

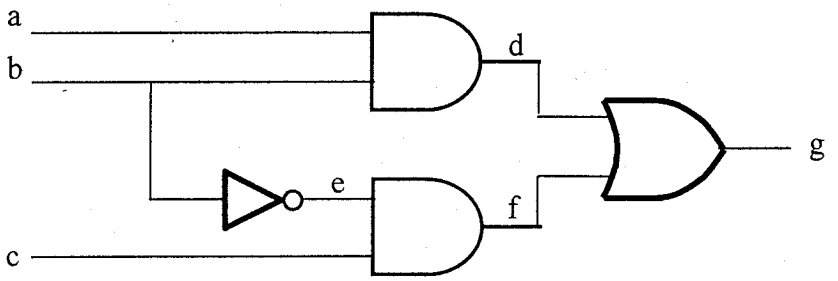

Figure 4a Combinational circuit to be tested

d) Explain how the circuit of figure 4c exhibits an undetectable stuck-at-0 fault on signal x (3 marks)

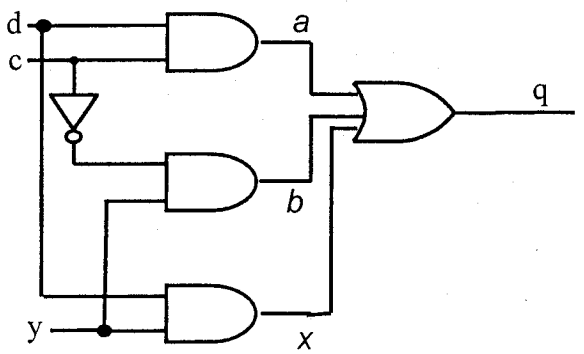

Figure 4c Combinational circuit to be tested

e) Illustrate a modification which makes the circuit of figure 4c testable. (2 marks)

f) The circuit of figure 4d describes a synchronous sequential state machine. Make this circuit testable by modifying it for scan path. Describe the resulting circuit operation. (4 marks)

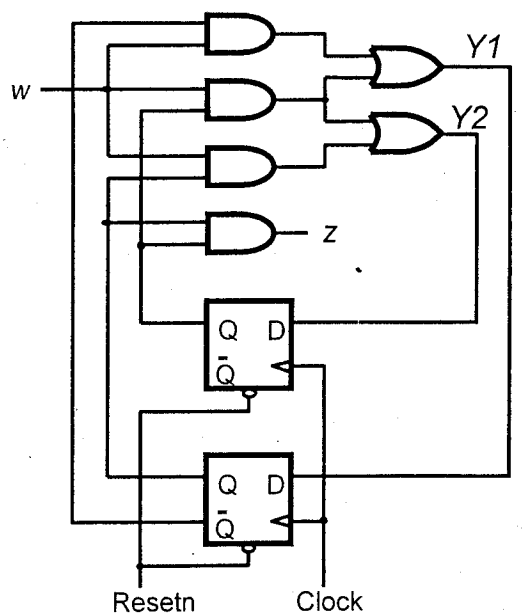

Figure 4d combinational circuit to be tested