

SEMESTER I EXAMINATIONS 2002/2003

B.Sc. (Honours) in  
Applied Physics & Electronics  
Experimental Physics

Paper II: Microelectronics (EP411)

4EL3-EP441-2, 4EL4-AX402-2  
4BS2-EP443-1, 4BS2-AX405-1  
1EM1-EP411-1

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Time allowed: TWO hours

Answer THREE questions.

Each question carries 33 marks.

Q.1 A silicon sample has a uniform donor doping of  $3 \times 10^{22} \text{ m}^{-3}$ .

(i) Calculate the total number of atoms  $Q$  deposited during a predeposition of p type doping using boron diffusion, for times,  $t$ , of (a) 1s, (b)  $2 \times 10^3 \text{ s}$ , and (c)  $10^4 \text{ s}$ . Use values for temperature,  $T = 1000^\circ \text{C}$ ; solid solubility,  $N_0 = 2 \times 10^{26} \text{ m}^{-3}$ ; diffusion coefficient  $D_1 = 2.7 \times 10^{-18} \text{ m}^2 \text{ s}^{-1}$  and

$$Q = N_0(4D_1t)^{1/2} / \sqrt{\pi} \text{ atoms m}^{-2}$$

[3,3,3 marks]

From a practical and economic point of view explain the significance of the three times chosen above, and describe the characteristics of the junction formed. [10 marks]

(ii) A limited source drive-in diffusion is now performed for  $T = 1100^\circ \text{C}$ ,  $D_2 = 3 \times 10^{-17} \text{ m}^2 \text{ s}^{-1}$  and time  $t = 3.6 \times 10^3 \text{ s}$ , and using the appropriate value of  $Q$ , from (i), calculate the junction depth following the drive-in. [14 marks]

Note: Useful expressions:  $Q/\sqrt{(\pi DT)}$  and  $\exp[-x^2/(4Dt)]$

Q.2 (i) In ion implantation explain the design rule that relates to the allowed value of dopant concentration in the tail of the distribution profile. [6 marks]

(ii) From (i) above and using a SiO<sub>2</sub> layer on doped Si, derive the equation  $x_0 = \text{minimum oxide thickness} = R_P + m \Delta R_P$ . Explain the significance of the value of m. [8 marks]

Note:  $N(x) = N_P \exp[-(x - R_P)^2 / 2\Delta R_P^2]$

(iii) A boron implantation is to be performed through a 50 nm gate oxide so that the peak of the distribution is at the Si - SiO<sub>2</sub> interface. The dose of the implant in silicon is to be  $1 \times 10^{13} \text{ cm}^{-2}$ , the peak concentration  $N_P = 3.5 \times 10^{18} \text{ cm}^{-3}$ , the straggle  $\Delta R_P = 0.023 \mu\text{m}$ , and the range  $R_P = 0.05 \mu\text{m}$ . How thick should the SiO<sub>2</sub> layer be in areas which are not to be implanted, if the background concentration is  $1 \times 10^{16} \text{ cm}^{-3}$ ? [11 marks]

(iv) In (iii) above, suppose the oxide is 50 nm thick everywhere. How much photo resist is required on top of the oxide to completely mask the ion implantation? Use a value of 1.8 as the stopping ratio for photoresist and SiO<sub>2</sub>. [8 marks]

Q.3 Explain the use of resists in lithography under the following headings:

(i) Initial criteria. [8 marks]

(ii) Image type. [6 marks]

(iii) Radiation type. [7 marks]

(iv) Process chemistry. [12 marks]

Q.4 Answer (a) and (b)

(a) The growth of SiO<sub>2</sub> on Si, during the oxidation process is given by the equation

$$\text{Oxide thickness} = d_{\text{ox}} = [A/2] \{ [1 + (t + \tau_o) / (A^2 / 4B)]^{1/2} - 1 \},$$

from which the growth time can be determined.

A 50 nm thick SiO<sub>2</sub> layer is first grown on top of the Si. Calculate the time t taken to grow an additional 0.2 μm thick SiO<sub>2</sub> film on top of the 50 nm SiO<sub>2</sub>, in wet oxygen at 1000°C.

At 1000°C for wet oxidation

$$B = 0.29 \mu\text{m}^2 \text{ h}^{-1}, B/A = 1.27 \mu\text{m h}^{-1} \text{ and } \tau_o = 0 \text{ h.} \quad [16 \text{ marks}]$$

(b) Using n-MOS gate circuits with a depletion load transistor, draw sketches of a two input NAND gate and a two input NOR gate. Briefly explain their operation.

Determine the channel lengths for the transistors in an n-MOS inverter made using a 3 μm process if the channel widths are to be equal. The voltage values for the fabrication process are  $V_{DD} = 5\text{V}$ ,  $V_{Tn} = 1.0\text{V}$ ,  $V_{TD} = -4.0\text{V}$ ,  $V_{LO} = 0.5\text{V}$ .

Assume  $\mu_n / \mu_D = 1.2$

(9, 8 marks)

Note:  $\beta_n V_{LO} (V_{DD} - V_{Tn} - V_{LO}/2) = \beta_D |V_{TD}|^2 / 2$

- Q.5 (i) Draw a vertical cross-section of the fabrication layout for a u.v. erasable MOST EPROM transistor and explain its WRITE and ERASE operation. [11 marks]
- (ii) Explain the design and use of programmable logic devices (PLDs) or user-configurable ICs (USICs). [10 marks]
- (iii) Draw the functional circuit for a PLD to implement the logic function

$$(\overline{A}.\overline{B}.C) + (\overline{A}.B.\overline{C})$$

using the MOST EPROMs as in (i) above.

Explain the circuit operation.

[6, 6 marks]