GK899

COLÁISTE NA hOLLSCOILE
GAILLIMH

NATIONAL UNIVERSITY OF IRELAND
GALWAY

SEMESTER 1 EXAMINATIONS 2002-2003

B.Sc. (Honours) Applied Physics and Electronics

Paper III: Digital Signal Processing (EP422)

4EL4-AX402-3, 4BS2-AX406-1
1EM1-EP422-1

Prof. E. Kennedy
Prof. S. G. Jennings
Dr J. Martin

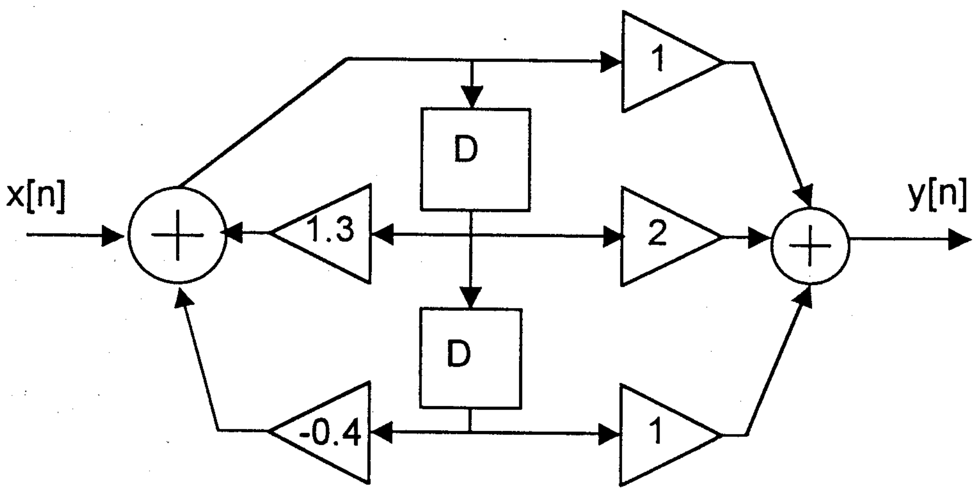
Time Allowed: TWO hours	Answer THREE questions

Q.1 State the *Sampling Theorem* and define the *DTFT* in Discrete Time (DT) systems. Prove the Sampling Theorem, by sketching typical (DTFT) frequency spectra of ideally sampled signals, or otherwise. Include an account of the phenomenon of *Aliasing* in sampled data systems, indicating how it arises and how it can be avoided. ***[5 marks]***

Explain fully the nature of the signal distortions introduced by the use of (a) a typical ADC (analog to digital converter) for sampling, and (b) a zero order hold DAC (digital to analog converter) for the reconstituted continuous time signal. How is the correction (or minimization) of the second type of distortion normally accomplished? ***[5 marks]***

Q.2 Briefly define or explain the following quantities as used in Discrete Time (DT) systems: (a) the impulse response h[n]; (b) the difference equation; (c) the transfer function H(z); and, (d) the Direct Form II (DF II) block diagram. Where appropriate, state how these quantities are inter-related. ***[4 marks]***

The DFII block diagram for a DT system, with input x and output y, is shown below. Find the expression for the system transfer function H(z), its difference equation, its poles and zeros, and say whether the system is stable or unstable. Calculate the numerical values of the first three terms in the impulse response of the system. ***[6 marks]***



Q.3 Say what is generally meant by a *digital filter*. State the relationship between the DT (Discrete Time) system function H(z) of a digital filter and its DT frequency response function H(ω). Explain how a pole-zero diagram of H(z) in the z-plane, together with the z-plane unit circle, are used to estimate the filter frequency response. ***[4 marks]***

Use the pole-zero technique, as explained above, to sketch the approximate (qualitative) magnitude responses for the following pole-zero plots. State also the type of the filter response (e.g., LPF, HPF, etc) produced in each case.

(a) Two poles at $z = \pm 0.9j$, and two zeros at $z = \pm 1$.
(b) One pole at $z = 0.5$ and one zero at $z = -1$.
(c) Six poles at the origin and five zeros on the z-plane unit circle, at angles of $60 \cdot n$ degrees to the real axis, where n = 1, 2, 3, 4, and 5. ***[6 marks]***

Q.4 Describe the three main techniques (Direct, Parallel, and Cascade) as used in practical DSP (Digital Signal Processing) systems to implement a general DT (Discrete Time) difference equation. Define what a Biquadratic Filter (BQF) stage is in your account. Briefly compare and contrast the relative advantages of the three approaches. ***[4 marks]***

Construct the section of TMS32010 assembly language code necessary to implement one BQF stage in a DSP system. Handle all input, output and intermediate signals, and also the difference equation coefficients, as Q15 fractions in your code. Estimate the execution time required for the stage. ***[6 marks]***

NOTE: A short TMS32010 instruction set is appended to this paper.

Q.5 Answer any *TWO* of the following. ***[5 marks each section]***

(a) Give a comparison of the BLT (Bilinear Transform) and II (Impulse Invariance) methods of DT system design, explaining how the BLT avoids the problem of aliasing. What is the disadvantage of the BLT approach compared to the II? How is this disadvantage partially overcome in practical design?

(b) Describe fully the window method of indirect digital filter design, explaining its suitability for the design of linear phase filters. Why is linear phase so desirable in practice?

(c) Write down the system function H(z) of a DT system with the following difference equation:

$$y[n] - 0.5y[n-1] = x[n] + 3x[n-1] + x[n-2]$$

Hence find the first three terms in the system impulse response by the two distinct methods of:

(i) a direct series expansion of H(z) using Long Division, and
(ii) a partial fraction expansion of H(z) followed by use of z-transforms.

Note that the z-transform of the exponential DT series $x[n] = a^n$ is $\frac{1}{1 - az^{-1}}$.

A short TMS32010 Instruction Set

A = 32 bit Accumulator

P = 32 bit Product register

T = 16 bit multiplicand register

Pan = I/O Port number n

d = Data memory address

S = Shift Left S bits

L = Label (address)

C = Constant

Mnemonic	Cycles*	Description
ABS	1	Absolute Value of A
ADD d,S	1	Add d (with shift) to A
AND d	1	AND d with A
APAC	1	Add P to A
B L	2	Branch unconditionally to label L
BGEZ L	2	Branch if A greater or equal to zero
BGZ L	2	Branch if A greater than zero
BIOZ L	2	Branch on BIO (I/O status) pin = 0
BLZ L	2	Branch if A less than zero
BLEZ L	2	Branch if A less than or equal to zero
BNZ L	2	Branch if A is not zero
BZ L	2	Branch if A is zero
CALL L	2	CALL subroutine L
DINT	1	Disable Interrupt
DMOV d	1	Copy contents of data memory d to next location
EINT	1	Enable Interrupt
IN d,PAn	2	Input data from I/O port n to d
LAC d,S	1	Load A from d (with shift)
LACK C	1	Load A with immediate 8 bit constant C
LT d	1	Load T from d
LTA d	1	Load T, add P to A (LT, APAC)
LTD d	1	Load T, add P to A, data move (LT, APAC, DMOV)
MPY d	1	Multiply d with T, store product in P
MPYK C	1	Multiply 13 bit constant C with T, product to P
NOP	1	No operation
OR d	1	OR d with A
OUT d,PAn	2	Output data from d to I/O port n
PAC	1	Copy P to A
RET	2	Return from subroutine CALL
SACH d,S	1	Store high order A (16 bits with shift) to d
SACL d,S	1	Store low order A (16 bits with shift) to d
SPAC	1	Subtract P from A
SOVM	1	Set Overflow Mode for A and ALU (±ve limits)
SUB d,S	1	Subtract d (with shift) from A
XOR d	1	Exclusive OR d with A
ZAC	1	Zero A

* **CPU cycle time** for the TMS32010 = 200 ns