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Ollscoil na hÉireann, Gaillimh
National University of Ireland, Galway

Semester II Examinations, 2004/2005

Exam Code(s)	2BN121 2BP121
Exam(s)	Second Year Electronic Engineering Second Year Electronic and Computer Engineering
Module Code(s)	EE211
Module(s)	Analogue Systems Design I
Paper No.	1
Repeat Paper	Special Paper
External Examiner(s)	Professor S. McLaughlin
Internal Examiner(s)	Professor D.J. Wilcox Dr. M. Duffy
Instructions:	Answer 5 questions. All questions carry equal marks.
Duration	3hrs
No. of Answer books	1
Requirements:	
Handout	
MCQ	
Statistical Tables	
Graph Paper	
Log Graph Paper	1
Other Material	
No. of Pages	5
Department(s)	Electronic Engineering

1.

(a) Sketch the I-V characteristic for a real diode and explain how it differs from that of an ideal diode. **[4 marks]**

(b) The input voltage in both circuits in Fig. 1 is $v_i(t) = 5 \text{ Sin } (100\pi t)$. **[9 marks]**

(i) Assuming ideal diodes, explain the operation of the half-wave rectifier in Fig. 1(a). Include a sketch of the output voltage waveform, $v_o(t)$.

(ii) Repeat part (i) for the full-wave rectifier in Fig. 1(b).

(iii) Show how $v_o(t)$ is changed in the half-wave rectifier of Fig. 1(a) if real diode properties are accounted for.

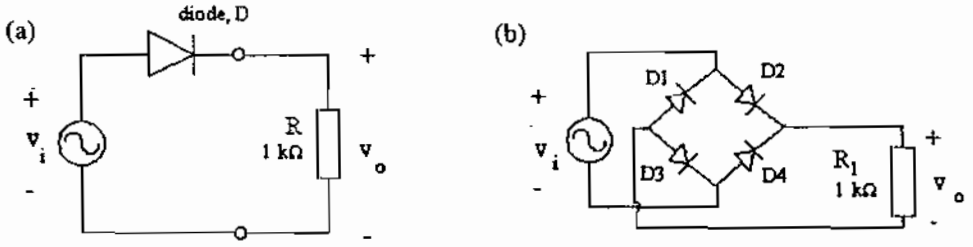


Fig. 1(a) Half-wave rectifier, (b) Full-wave rectifier

(c) Explain the operation of the clamping circuit shown in Fig. 1(c) for an input sinusoid, $v_s(t)$, with 25 V amplitude and 1 kHz frequency, and with V_B = 10 V. Include a sketch of the output voltage waveform, $v_o(t)$ to illustrate your answer. **[7 marks]**

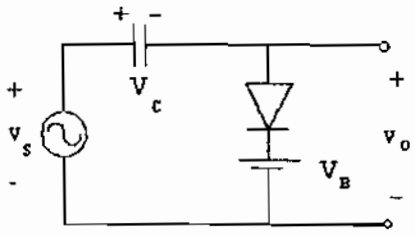


Fig. 1(c) Diode clamping circuit

2.

(a) Describe the 3 operating modes of a Bipolar Junction Transistor (BJT). **[5 marks]**

(b) Using the *exact* method of calculation, determine the DC bias values of V_B, V_C, V_E, I_B, I_C and I_E in the circuit of Fig. 2. **[10 marks]**

(c) Calculate (i) the AC voltage gain and (ii) the power consumption of the circuit in Fig. 2. **[5 marks]**

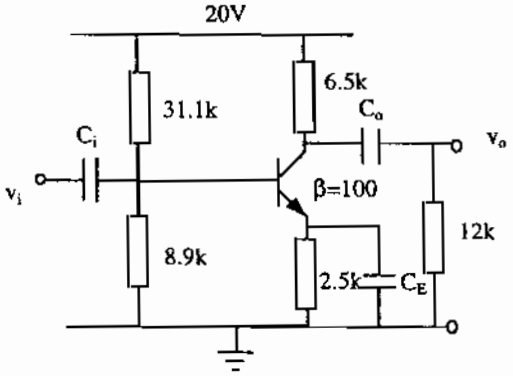


Fig. 2 Common emitter amplifier circuit

Contd.

3.

(a) Describe the semiconductor make-up of an n-channel Junction Field Effect Transistor (JFET), and explain the shape of the typical JFET characteristic curves shown in Fig. 3(a). **[8 marks]**

(b) Given values of I_{DSS} = 8 mA and $V_{GS(off)}$ = –6 V for the JFET in the circuit of Fig. 3(b), calculate the DC bias values of V_{GS}, V_D and I_D in this case. **[12 marks]**

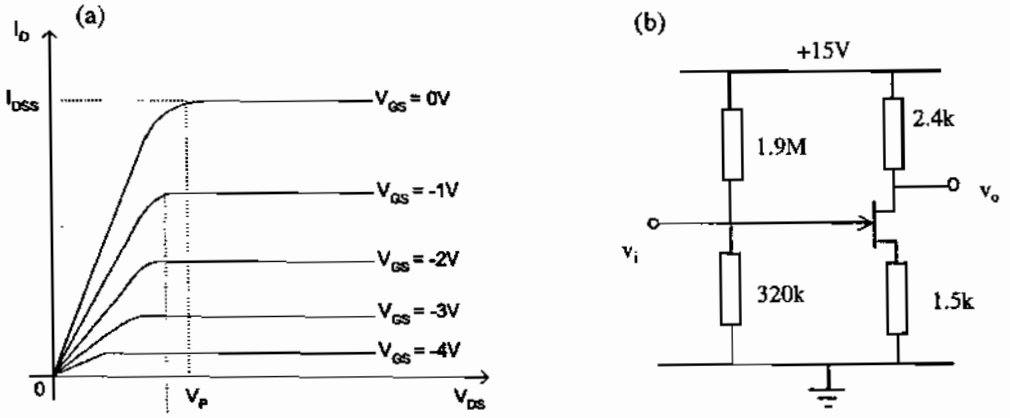


Fig. 3 : (a) JFET characteristic I_{DS} vs. V_{DS} curves, (b) JFET bias circuit

4.

(a) Complete the Box Model for the emitter follower circuit shown in Fig. 4. **[13 marks]**

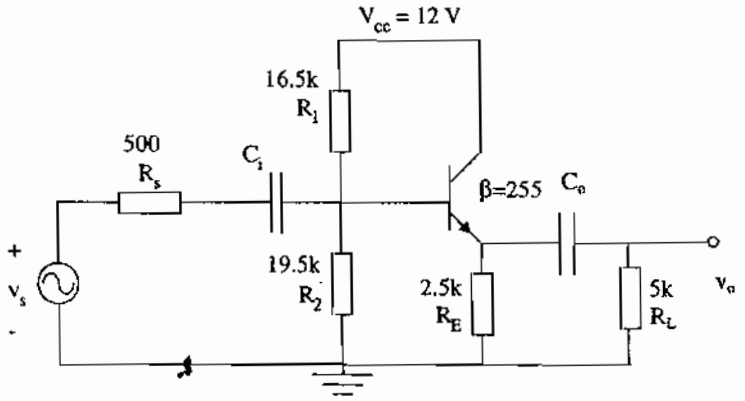


Fig. 4 : Emitter follower circuit

(b) With the source and load connected : **[5 marks]**

(i) Calculate the system gain, A_{sys}.

(ii) Plot two periods of the output voltage, $v_o(t)$, for $v_i(t) = 0.2\text{Sin}(100\pi t)$ V.

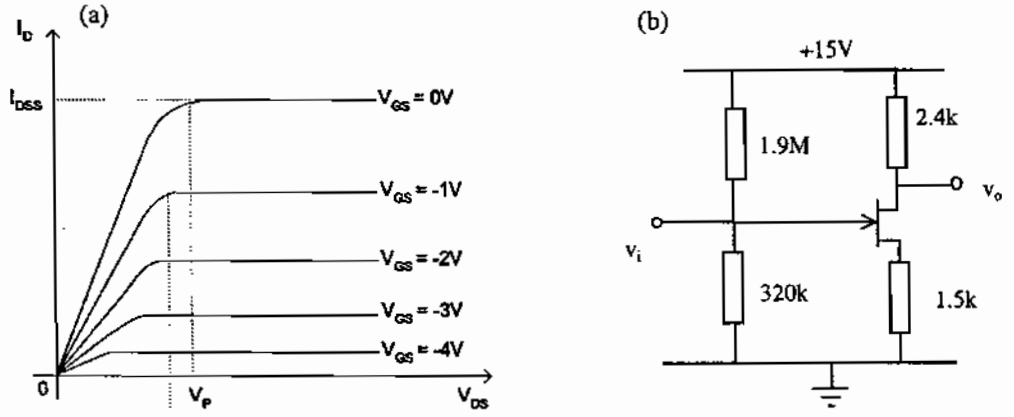
(c) Comment on the performance of the emitter follower as a unity gain buffer amplifier in this case. **[2 marks]**

Contd.

3.

(a) Describe the semiconductor make-up of an n-channel Junction Field Effect Transistor (JFET), and explain the shape of the typical JFET characteristic curves shown in Fig. 3(a). **[8 marks]**

(b) Given values of I_{DSS} = 8 mA and $V_{GS(off)}$ = −6 V for the JFET in the circuit of Fig. 3(b), calculate the DC bias values of V_{GS}, V_D and I_D in this case. **[12 marks]**



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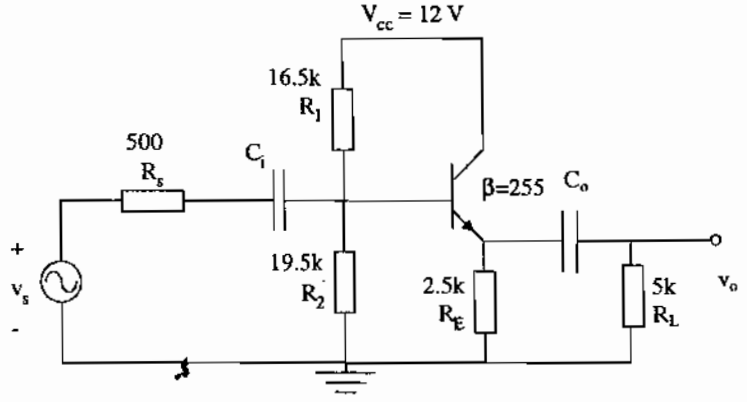

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(b) With the source and load connected : **[5 marks]**

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Contd.