956

Ollscoil na hÉireann, Gaillimh
National University of Ireland, Galway

Semester II Examinations, 2004/2005

Exam Code(s)	4BN121, 4BP121
	Degree : Electronic Engineering
	Degree : Electronic & Computer Engineering
Exam(s)	Digital Systems Design & VHDL
Module Code(s)	EE427
Paper No.	2
Repeat Paper	Special Paper
External Examiner(s)	Professor S. McLaughlin
Internal Examiner(s)	Professor D.J. Wilcox
	Dr. F. Morgan
Instructions:	Answer three questions All questions carry equal marks. *Candidates should note that marks may be lost if answers are not presented in a neat and legible format* *Where applicable, include rough-work calculations to obtain full marks for questions*
Duration	2 hrs
No. of Answer books	1
Requirements:	
Handout	
MCQ	
Statistical Tables	
Graph Paper	
Log Graph Paper	
Other Material	
No. of Pages	9
Department(s)	Electronic Engineering

Q1

Figure 1a (final page of paper) illustrates a block diagram for a single cycle computer system. The diagram highlights control and datapaths.

a Define a clear and complete signal data dictionary for each Program Counter Control Unit input and output signal
[include signals JMP, zeroFlg, endProg, execInstr, clk, rst, PCOffset, PC] **4 marks**

b Referring to the data dictionary, describe how these signals control each mode of operation of the Program Counter Control Unit **3 marks**

c Create a synthesisable VHDL model for the Program Counter Control Unit **6 marks**

d Figure 1b illustrates the symbol for an 8-bit barrel shifter

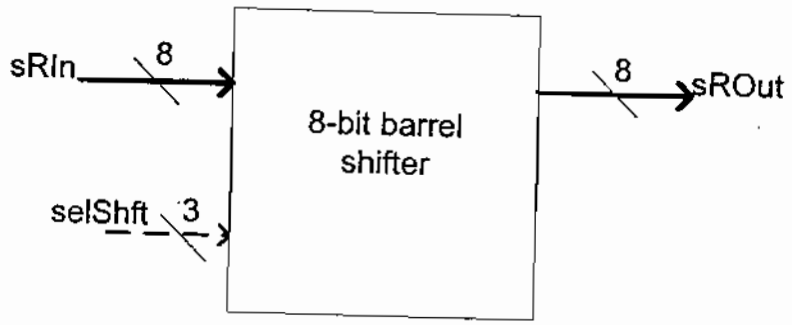

Figure 1b An 8-bit barrel shifter symbol

e List a complete function table for the barrel shifter. **3 marks**

f Write a synthesisable VHDL model for the incomplete process in listing 1a to describe the 8–bit barrel shifter. Recommendation : do NOT use a for loop. **4 marks**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity barrelShftr8Bit is
    Port ( sRIn : in std_logic_vector(7 downto 0);
           sROut : out std_logic_vector(7 downto 0);
           selShft : in std_logic_vector(2 downto 0));
end barrelShftr8Bit;

architecture comb of barrelShftr8Bit is
begin

-- complete code for process
shftProc: process

end process;

end comb;
```

Listing 1a : 8-bit barrel shifter VHDL model template.

Q2.

Figure 2a illustrates the function table for the Arithmetic and Logical Unit (ALU) element of the single cycle computer (of fig 1a). Figure 2b illustrates the ALU Adder X-input logic function table.

FS(2) [sel(2)]	*FS(3) [Cin]*	*FS(1:0) [sel(1:0)]*	*ALUOut*	*Function*
0	0	00	aBus	transfer aBus
0	1	00		
0	0	01		
0	1	01		
0	0	10		
0	1	10		
0	0	11		
0	1	11		
1	X	00		
1	X	01		
1	X	10		
1	X	11		

Figure 2a ALU Function Table

	FS(1:0) [sel(1:0)]	X
ALU Adder X i/p logic function table	00	all 0's
	01	bBus
	10	bBus
	11	all 1's

Alias signal names for FS(4:0)
Cin=FS(3)
sel(2:0)=FS(2:0)

Figure 2b ALU Adder X-input logic function table

a Complete the Function table of fig 2a, including each ALUOut signal value for each FS(3:0) input signal combination. Refer to fig1a as required to derive this information **8 marks**

Figure 2c illustrates a 5-bit binary multiplier block diagram.

b Design a suitable Multiplier Datapath Transfer Unit. **6 marks**

c Explain the requirement and operation of each element of the multiplier. **3 marks**

d Design a flowchart describing the behaviour of the ASM unit. Include a key. **3 marks**

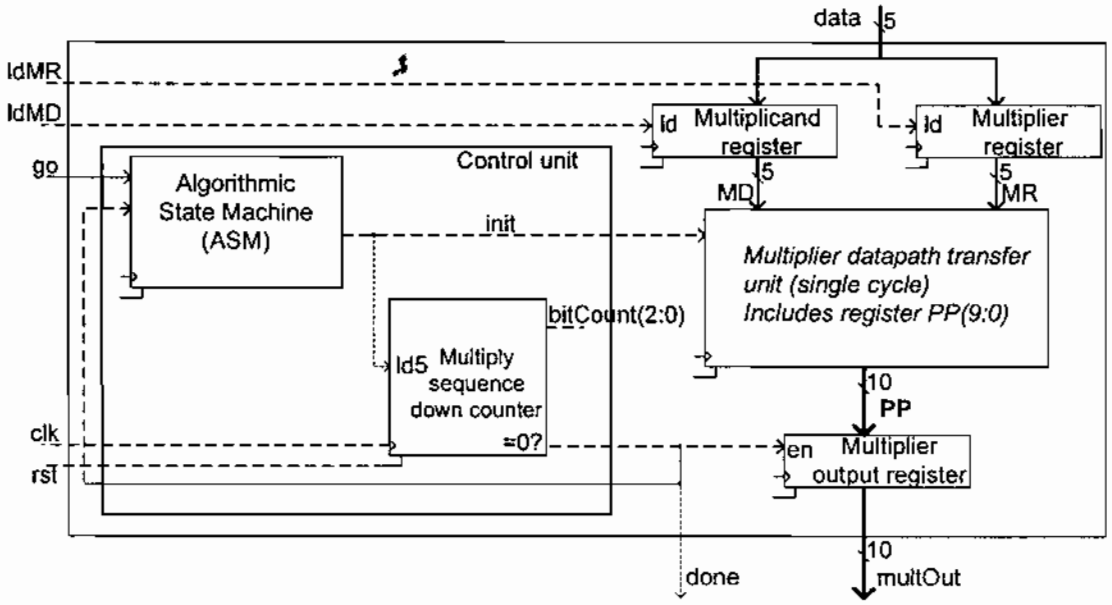

Figure2c 5-bit binary multiplier block diagram

Q3.

a Define the fundamental mode rule as applied to asynchronous sequential system behaviour. How is this rule manifested by manufacturers in typical devices provided for use in synchronous circuit designs ? **2 marks**

b Describe the meaning of a static-0 hazard. Illustrate with a timing diagram. Describe a technique which can be used to detect the existence of a static hazard in a logic circuit and to ensure that the hazard is removed. **2 marks**

The circuit of fig 3a describes an asynchronous sequential system.

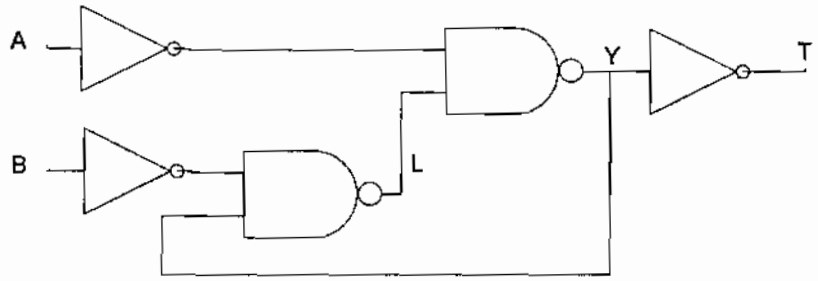

Fig 3a Asynchronous state machine circuit diagram

c Use a clear reverse engineering methodology to generate a minimal state diagram representing the functionality of the circuit. Include input & output signal values and state names on the state diagram and a key explaining the state diagram format. **6 marks**

d Use the state transition diagram derived in part c to complete the timing diagram of fig 3b [Fig 3b is also included on a separate page which may be submitted with the exam script] **2 marks**

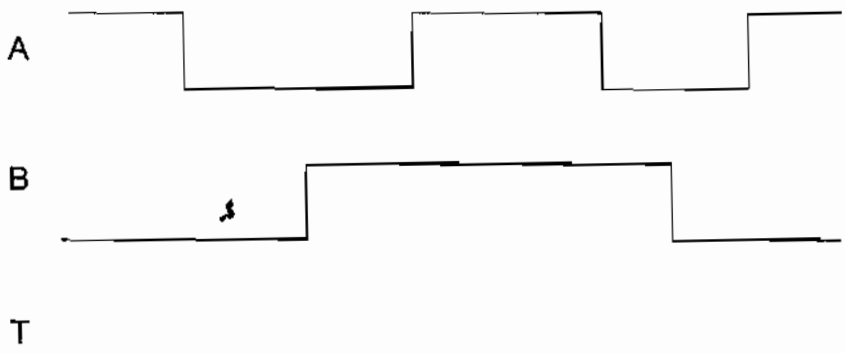

Fig 3b Asynchronous state machine timing diagram (to be completed)

The timing diagram of figure 3c illustrates the behaviour of an asynchronous sequential system. Inputs : X_1 , X_0 Output : Z

e Design an asynchronous sequential circuit to implement the system **8 marks**

Ensure that you use the full timing diagram in figure 3c in your analysis. Use a clear design & documentation methodology.
[Fig 3c is also included on a separate page which may be submitted with the exam script]

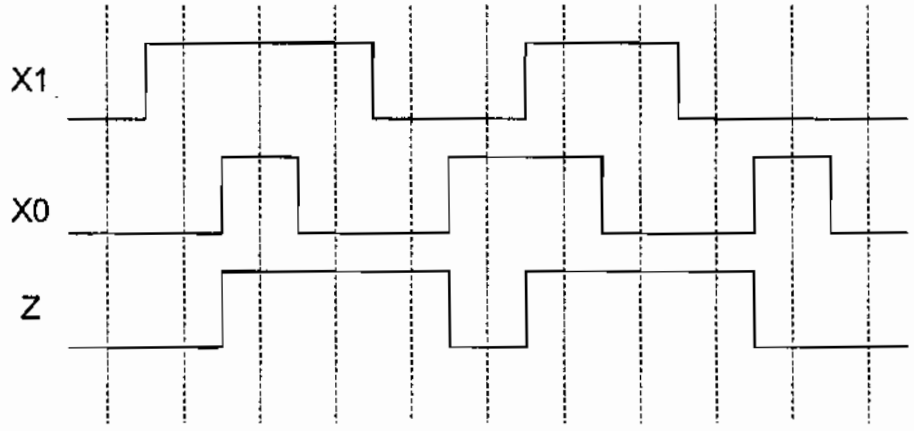

Fig 3c Asynchronous sequential system timing diagram

Q4.

a Draw a detailed functional partition illustrating a dedicated multiplexer-based datapath transfer architecture . Include all signal names and explain its operation. **3 marks**

b i) Draw a detailed functional partition illustrating a tri-state bus transfer architecture. Include all signal names and explain its operation. **3 marks**

ii) Create a synthesisable VHDL model for the tri-state bus transfer implementation. Use the same signal names as in part 4b(i) **6 marks**

c Explain the operation of each part of the circuit test structure (figure 4a) and reason for its usage. **3 marks**

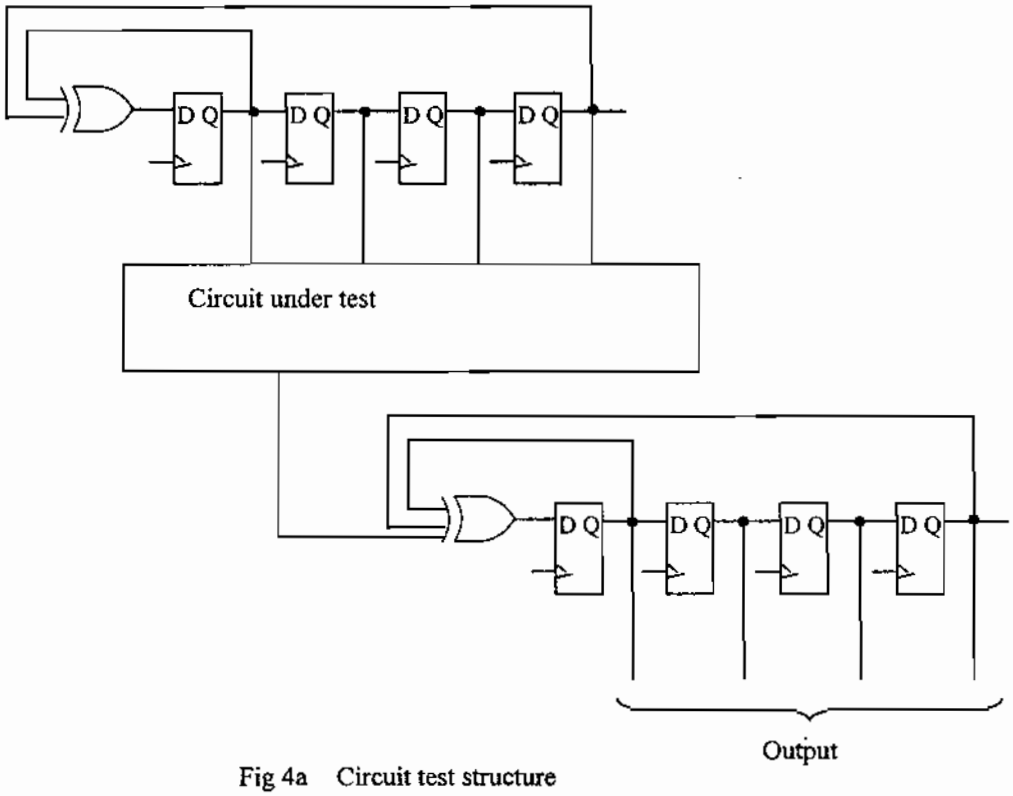

Fig 4a Circuit test structure

d A partially completed fault detection table for the combinational circuit of figure 4b is illustrated in fig 4c (see attached sheet at end of examination paper). Complete the fault detection table and derive a minimal test vector set for the circuit. **5 marks**
Submit figure 4c with your answer sheet. Include your detailed test set derivation work.

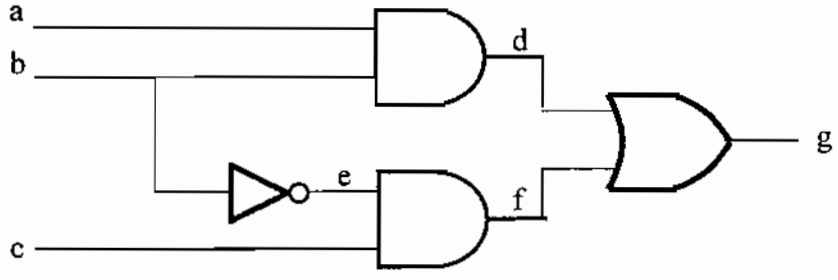

Figure 4c Combinational circuit to be tested