GX550

OLLSCOIL NA hÉIREANN, GAILLIMH
NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS, 1999

FIRST ELECTRONIC ENGINEERING
FIRST ELECTRONIC AND COMPUTER ENGINEERING
SECOND INDUSTRIAL ENGINEERING

DIGITAL ELECTRONICS

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Duration of examination: *Two* hours

Instructions: Answer *four* questions

1. **(a)** **(i)** Describe in your own words the fundamental difference between a digital and an analogue electronic circuit. [2 marks]

(ii) Explain with the aid of diagrams the function of a *tri-state buffer* in a digital logic circuit. [5 marks]

(iii) List the seven basic digital logic gates and give the truth table for each gate. [4 marks]

(iv) Show how it is possible to construct a logical AND gate using two diodes and a resistor. Give an explanation of how this circuit works for all possible inputs. [5 marks]

(b) The circuit of figure 1 below shows a combinational logic circuit.

(i) Write down the truth table for this circuit. [3 marks]

(ii) Determine the Boolean expression describing this system. [3 marks]

(iii) Give a minimal expression for F. [4 marks]

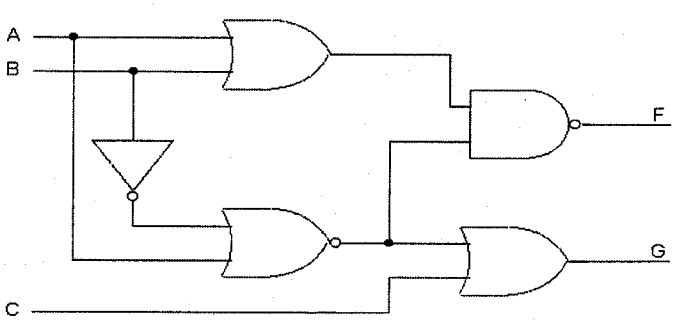

Figure 1.

2. **(a)** Using the laws of Boolean Algebra minmise the following expressions:

(i) $F = \overline{A}B\overline{C} + \overline{A}BC + ABC$ [4 marks]

(ii) $F = AB\overline{C} + ABC + A\overline{B}\overline{C} + A\overline{B}C$ [4 marks]

(iii) $F = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC$ [4 marks]

(b) Use Karnaugh mapping to minimise each of the following expressions:

(i) $F = \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + AB + A\overline{B}C$ [4 marks]

(ii) $F = AB\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}BCD + AB\overline{C}\overline{D}$ [4 marks]

(c) Determine the Boolean logic expression described by the Karnaugh map below and give a circuit implementation of the expression:

Y	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	0	1	1	0
$\overline{A}B$	1	0	0	1
AB	1	0	0	1
$A\overline{B}$	0	1	1	0

[5 marks]

3. **(a)** Convert the following numbers to decimal clearly showing the conversion technique used in each case.

(i) 10010110_2 [2 marks]

(ii) $3E5_{16}$ [3 marks]

(iii) 54.74_8 [3 marks]

(b) Convert each of the following numbers to hexadecimal format showing clearly the conversion technique used in each case.

(i) 10010110_2 [2 marks]

(ii) 478_{10} [3 marks]

(iii) 456.5_8 [5 marks]

(c) Convert the following Gray coded numbers to their equivalent BASE-2 binary format and show how they would be subtracted using two's compliment arithmetic

$1110_{GRAY} - 0110_{GRAY}$ [7 marks]

4. **(a)** **(i)** The diagram of figure 4.1 shows a sequential logic circuit which can act as a single bit memory element. Complete the truth table for this circuit, indicating all possible outputs Q_{n+1} for all possible combinations of inputs and previous outputs Q_n. [4 marks]

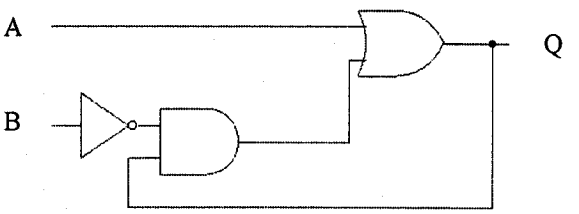

Figure 4.1

(ii) State which inputs **Set** and **Reset** the memory element. [2 marks]

(iii) State for which input combination is the device acting as a single bit memory. [2 marks]

(b) The diagram of figure 4.2 shows an S-R flip-flop. If the waveforms shown in the figure are applied to the S and R inputs sketch the waveforms of the Q and $\overline{Q}$ outputs. [6 marks]

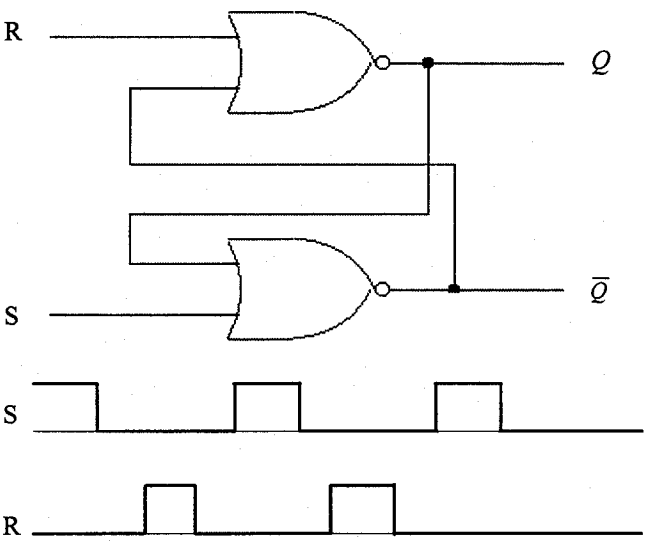

Figure 4.2

(d) (i) Show how two S-R flip-flops can be connected together with additional circuitry to form a master-slave J-K flip-flop. [6 marks]

(ii) Describe how it is possible to use this flip-flop in toggle mode and design a circuit using J-K flip-flops that can generate two clock outputs of frequency 4khz and 8kHz from an input clock of frequency 16kHz. [5 marks]

5. You a required to design a combinational logic circuit for a process monitoring system. The circuit will be connected to a number of sensors (A, B, and C) and will have two outputs (X and Y).

Sensor A: Emits a HIGH if a CO_2 gas is detected.

Sensor B: Emits a HIGH while process is active.

Sensor C: Emits a 3 bit binary number which is directly proportional to the pressure in gas chamber.

In normal operation the pressure indicator should read between 4 and 7 (inclusive) while the process is active and between 2 and 6 (inclusive) when the process is inactive.

Output X: This is an Abnormal Pressure Alarm signal, which should go HIGH if the pressure is outside its normal ranges.

Output Y: This is a CO_2 Gas Alarm signal, which should go HIGH if CO_2 gas is detected when the process is inactive and at the same time the pressure is at an abnormal level.

Design the combinational logic circuit for the system.
Your design should include truth tables, Karnaugh Mapping minimisation and circuit implementation using **NAND** gates only.

[25 marks]

6. Answer any **TWO** parts.

(a) Design a synchronous sequential logic counter which will count in the following sequence: 1, 3, 5, 7, 9, 11, 13, 1, 3 ... [12.5 marks]

(b) Design a combinational logic circuit which will have two inputs A and B. Both A and B are two bit numbers. The circuit is to have a single output which will be HIGH if the product of the numbers A and B is even. Note that Zero is considered odd. Your design should include a truth table, minimisation and circuit implementation using **NOR** gates only.

[12.5 marks]

(c) Draw the truth table for a full adder which will add two single bit numbers X and Y a and a input carry bit C_{in} to give sum and carry outputs S and C_{out}. Write down Boolean expressions for the two outputs and proceed to express them in minimal form. Give a circuit implementation for the adder based on the minimal expressions.

[12.5 marks]