GX558

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THE NATIONAL UNIVERSITY OF IRELAND, GALWAY

SUMMER EXAMINATIONS 1999

B.E. DEGREE IN ELECTRONIC ENGINEERING

MICROELECTRONICS AND VLSI DESIGN

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Duration of Examination : **3 hours**

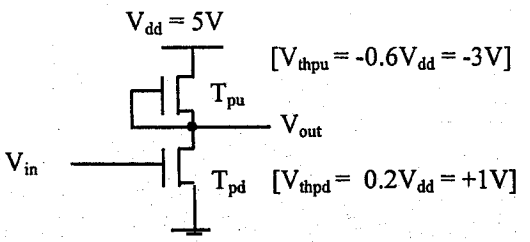
Instructions — Answer **FIVE** questions.
All questions carry equal marks.

1. a) Sketch and explain the 'ideal' inverter transfer characteristic (2 marks)

b) Sketch the following nMOS inverter circuits and corresponding transfer characteristics and illustrate their limitations relative to the ideal inverter.
i) enhancement mode pulldown transistor and pullup resistor (2 marks)
ii) enhancement mode pulldown and pullup transistors (2 marks)
iii) enhancement mode pulldown transistor and depletion mode pullup transistor (2 marks)

c) Illustrate the effect of decreasing the Z_{pu}/Z_{pd} ratio on the inverter characteristic. (2marks)

d) Assuming Zpu/Zpd = 4 for the nMOS inverter of figure 1(a), calculate the low output voltage. Assume t_{ox} is the same for both transistors. (5 marks)



$$I_{ds}(lin) = \mu.C_{ox}\frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^{2}\right]$$

$$I_{ds}(sat) = \mu.C_{ox}\frac{W}{2L}\left(V_{gs} - V_{th}\right)^{2}$$

Figure 1(a)

e) If Zpu/Zpd = 1, calculate the inverter switching voltage, V_{inv} (5 marks)

2. a) Illustrate how the CMOS inverter offers improvements over nMOS-only technology (3 marks)

b) Outline the 5 distinct regions of operation of the CMOS inverter. Support using voltage transfer and current characteristics.
Describe the mode of operation of the transisitors in each region. (3 marks)

c) Briefly outline the typical CMOS fabrication process steps. Illustrate with sketches. (6 marks)

d) Sketch and explain the basic operation and application of a conventional BiCMOS inverter circuit. (4 marks)

e) Describe latchup in BiCMOS circuits. Outline two methods used to minimise the occurrence of latchup (4 marks)

3. a) Design a CMOS combinational logic circuit to implement the following function:

$$F = \left(A.\overline{B} + C\right)\left(A + \overline{B}.D\right)$$ (5 marks)

Do not attempt any minimisation.

b) Draw the equivalent coloured mask stick diagram for the CMOS mask layout of figure 3(a) below. [Input signals : X,Y,Z,B. Output signal S] (5 marks)

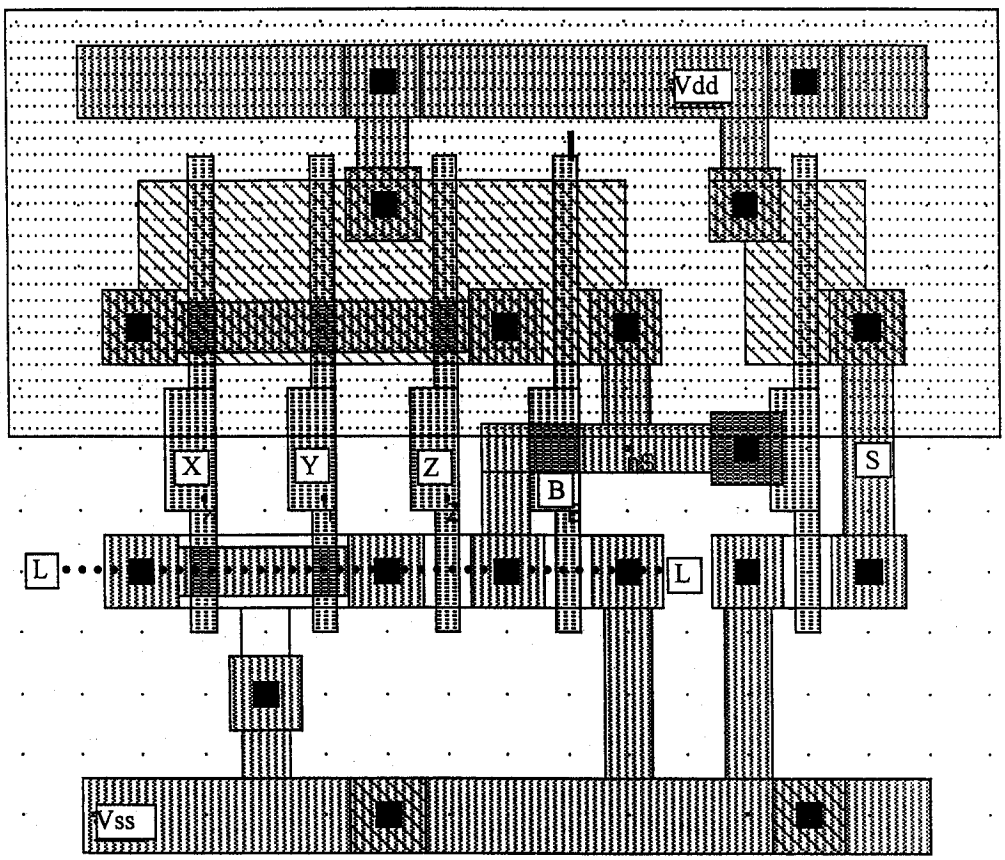


Figure 3(a) CMOS circuit mask layout

c) Draw the MOS transistor level circuit diagram for the CMOS implementation of figure 3(a) and derive the boolean description for the circuit (5 marks)

d) Sketch the device layer profile for the section through the line L---L in figure 3(a). Label all regions (e.g., silicon type, SiO_2 (gate & field), gate, metal etc). (3 marks)

e) Illustrate the advantage that can be gained by implementing a CMOS logic circuit using NAND gates rather than NOR gates ? (2 marks)

4. a) Describe the operation of a CMOS transmission gate and comment on how it is superior to nMOS and pMOS pass transistors. (4 marks)

b) A 4-to-1 multiplexer with input data lines D0, D1, D2, and D3 uses 2 select signals S0 and S1 to direct a selected data line to a single output F and may be described by the following function:

$$F = S_0 S_1 D_0 + S_0 \overline{S_1} D_1 + \overline{S_0} S_1 D_2 + \overline{S_0 S_1} D_3$$

Design a transmission gate based circuit to implement the multiplexer, using the select signals to control conduction through the transmission gates. Label all signals (6 marks)

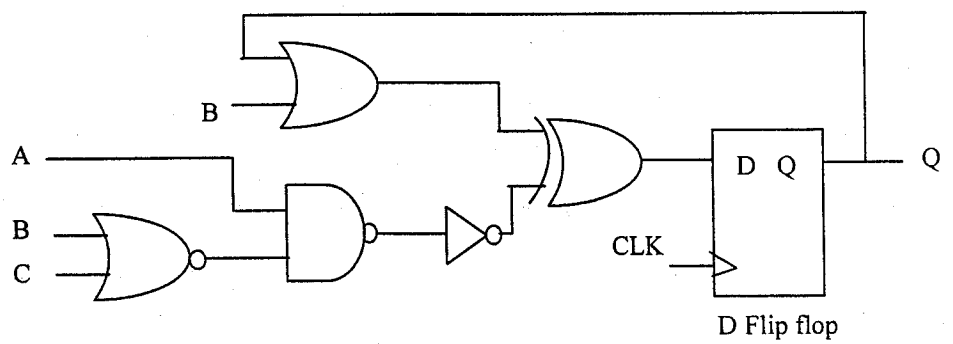
c) Calculate the CMOS inverter switching voltage (V_{INV}) for the following CMOS inverter transistor parameters :
$V_{thpd}=-V_{thpu}=1V$, $W_{pd}/L_{pd}=2$, $W_{pu}/L_{pu}=8$, $\mu_n=2\mu_p$, $V_{dd}=5V$
Clearly state (and verify) transistor operation modes
(7 marks)

d) Calculate the CMOS inverter current at the inverter switching point.
$K_{pd}=\mu C_{ox} = 20\mu A/V^2$ (3 marks)

5. a) Describe the uses and benefits of VHDL. (3 marks)

b) Discuss the differences between signals and variables in VHDL (3 marks)

c) Write a VHDL description for the following sequential circuit using concurrent statements and process. Each gate has a 5ns delay, excluding the inverter which has a 2ns delay.
(8 marks)



D Flip flop

d) What value will vectors A, B, C and D be given after the following assignments ? (6 marks)

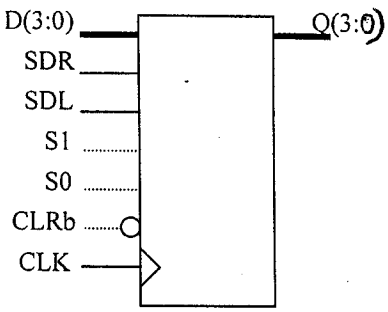
```
Architecture RTL of EX3 is
signal A, B : std_logic_vector(4 downto 0);
signal C    : std_logic_vector(0 to 1);
signal D    : std_logic;
begin

 Proc1 : Process Q (B,C,D)
 variable V : std_logic;
 begin
   V := '1';
   A <= (1=>'0', 3=> V, others => B(2));
   D <= '1', V:= '0';
   B <= (1=>D, 3=> V, others => C(1));
   D <= '0';
   C <= "10";
 end process;

end RTL;
```

6. A description of a 74194 four-bit bidirectional shift register follows :

CLRb	CLK	S1	S0	Q(3:0)	Description
L	X	X	X	0000	Async reset
H	↑	1	1	D(3:0)	Parallel Load
H	↑	1	0	SDR, Q(3:1)	Shift right, SDR shifted into Q(3)
H	↑	0	1	Q(2:0), SDL	Shift left, SDL shifted into Q(0)
H	↑	0	0	Q(3:0)	No action



a) Write a behavioural VHDL model for the 74194 (10 marks)

b) The VHDL model of figure 7.2 describes a sequential system. The port names have been changed to obscure the model functionality. Examine the VHDL model and draw the detailed functional block diagram
What is the exact function of the VHDL model ? (6 marks)

```
entity WHAT_IS_THIS is
  port(
    di: in std_logic_vector(3 downto 0);
    clk, rst, sigIn1 : in std_logic;
    sigOut1: out std_logic;
    dO: out std_logic_vector(3 downto 0)
  );
end WHAT_IS_THIS;

architecture RTL of WHAT_IS_THIS is
signal cs : std_logic_vector(3 downto 0);
signal ns : std_logic_vector(4 downto 0);

begin
  ns <= ('0' & cs) + "01";

  PROC1: process(clk, rst)
    begin
      if (rst = '1') then
        cs <= (OTHERS => '0');
      elsif (clk'event and  clk = '1') then
        if (sigIn1 = '1') then
          cs <= di;
        else
          cs <= ns(3 downto 0);
        end if;
      end if;
  end process PROC1;

  -- Assign output values
  dO <= cs;
  sigOut1 <= cs(0) AND cs(1) AND cs(2) AND not cs(3);
end RTL;
```

Figure 6.2

c) Describe, with the aid of diagrams, the main elements in the Xilinx XC4000 device architecture (4 marks)

7. A switch debounce system timing diagram is illustrated in figure 5(a). The system senses the state of the switch input [SW(h)] and, if high, asserts output signal DEB for exactly one clock cycle irrespective of how long SW(h) remains asserted. The system does not allow additional assertions of DEB until SW(h) is first deasserted.

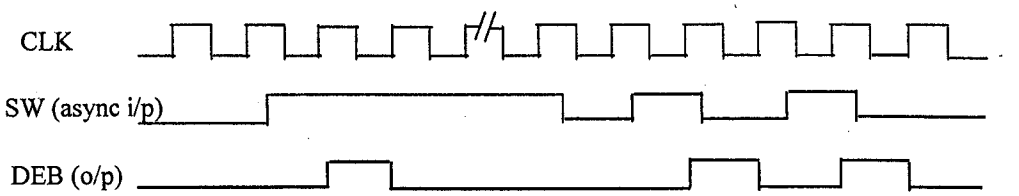


Figure 5(a)

a) Draw the flow chart describing the debounce system behaviour (include key indicating use of latched/unlatched signals). Re-draw the timing diagram labelling each state transition. (5 marks)

b) Write a VHDL model for the debounce system (entity and architecture sections). (7 marks)

c) Comment on the circuit resulting from synthesis of the following VHDL model : (3 marks)

```
LIBRARY section ..
entity ABC is port (a, b, sela, selb    :in std_logic; q : out std_logic); end ABC;
architecture BEHAVE of ABC is
begin
  PROC1: process (a, b, sela, selb)
     begin
          if sela = '1' then q <= a;  elsif selb = '1' then q <= b; end if;
     end process;
END behave;
```

d) Draw the logic diagram resulting from synthesis of the following code (5 marks)

```
entity UNK is
    port  (a, b, enable, clk, sel        :in std_logic;  gatedq :out std_logic);  end UNK;
architecture RTL of UNK is
signal inter, edge, q          :std_logic;
begin
     inter <= a when sel = '0' else b;
     edge <= enable and clk;
     CONNECT: process (edge)
     begin
          if (edge'event and edge = '1') then
               q <= inter;
          end if;
     end process CONNECT;
     gatedq <= q and enable;
end RTL;
```